IET Power Electronics

Research Article

ISSN 1755-4535
Received on 29th September 2014
Revised on 10th February 2015
Accepted on 28th April 2015
doi: 10.1049/iet-pel.2014.0746
www.ietdl.org

Structure of boost DC-link cascaded multilevel inverter for uninterrupted power supply applications

Ramasami Uthirasamy[1] ✉, *Uthandipalayam Subramaniyam Ragupathy*[2], *Venkatachalam Kumar Chinnaiyan*[3]

[1]*Department of EEE, Jansons Institute of Technology, Coimbatore, India*
[2]*Department of EIE, Kongu Engineering College, Erode, India*
[3]*Department of EEE, Dr. NGP Institute of Technology, Coimbatore, India*
✉ *E-mail: rusamy83@jit.ac.in*

Abstract: In this study, a structure of single-phase seven-level boost DC-link cascaded multilevel inverter (BDCLCMLI) is proposed. It consists of boost converter, DC-link module and H-bridge inverter. Compared with conventional CMLI and two level H-bridge inverter configurations, the proposed system results in reduction of voltage stress across the inverter switches, reduced power switches, DC source count and gate drive requirements. DC-link switching is achieved by multicarrier sinusoidal pulse-width modulation technique which results in improved quality of obtained output AC power. Reduction in DC source and switch count makes the system more cost effective. A simulation and prototype model of seven-level BDCLCMLI system is developed and its performance is analysed for various operating conditions.

1 Introduction

In recent years, power converters have been one of the most active areas of research in power electronics. Different families of power converters have been designed to interface the renewable resources for uninterrupted power supply (UPS) applications. Multilevel inverters (MLIs) are emerging as the new breed of power converter options for high-power applications [1, 2]. The three different topologies of MLI are diode clamped MLI, flying capacitor MLI (FCMLI) and cascaded multilevel inverter (CMLI [3, 4]. CMLI synthesises the staircase AC voltage waveform from several DC sources with reduced harmonic content [5]. Therefore the CMLI configuration is more attractive than other two configurations. The structure of CMLI is shown in Fig. 1*a*.

To obtain the nominal output voltage in CMLI, multilevel boost chopper is proposed in between the DC sources and H-bridges instead of magnetic components such as transformer [6, 7]. The efficiency and handling of CMLI and boost CMLI (BCMLI) configurations [8] are degraded because of more number of controlled power switches and DC sources. The structure of BCMLI is shown in Fig. 1*b*. Therefore certain modifications can be made in conventional CMLI and BCMLI systems [9–13]. In the proposed system, the nominal output voltage is obtained by introducing the boost chopper circuit in between the DC sources and DC-link inverter. The DC input voltage is boosted to the nominal voltage level by the boost chopper network. This results in reduction of number of DC sources and power switches.

In this paper, a single-phase seven-level asymmetrical source boost DC-link CMLI (BDCLCMLI) system is developed for UPS applications. The general structure of the proposed BDCLCMLI system is shown in Fig. 1*c*. To obtain better quality of AC power (with reduced harmonic content), multicarrier sinusoidal pulse-width modulation (MCSPWM) switching strategy is developed for DC-link switches [14–24]. This paper is organised into six sections as follows: motivation of boost chopper is reviewed in Section 1. Structure of BDCLCMLI system is addressed in Section 2. MCSPWM switching technique is reviewed in Section 3. Realisation of hardware prototype model is described in Section 4. Performance analysis of BDCLCMLI system is detailed in Section 5 and Section 6 concludes this paper.

2 Structure of BDCLCMLI system

BDCLCMLI system consists of two asymmetrical DC voltage sources, boost chopper unit, DC-link module (DCLM) and H-bridge inverter. H-bridge inverter is connected in parallel to the DC-link system.

2.1 Boost DC-link configuration

Each boost chopper unit is connected with asymmetrical DC sources and each DCLM consists of two power semiconductor switches whose output voltage is always unidirectional. The equivalent structure of BDCLCMLI is shown in Fig. 1*d*.

Number of levels in BDCLCMLI configuration is calculated as

$$N_{\text{level}} = 2(m+1)^S - 1 \tag{1}$$

Number of switches in BDCLCMLI is given by (2)

$$N_{\text{Switch}} = 2s + 4m + n \tag{2}$$

where N_{level}-number of levels, N_{Switch}-number of switches in BDCLCMLI, m-number of H-bridge inverter, s-number of DC sources and n-number of boost chopper units.

2.2 Modes of operation

2.2.1 Operation of boost DC-link configuration: To obtain seven-level AC output from two asymmetrical DC sources, the proposed system can be operated for six modes of operation.

Modes 1 and 4 operations: In modes 1 and 4 operations, the source voltage V_{dc1} is boosted to V_{ob1} by activating the boost chopper switch S_a and the conducting DC-link switches are S_6 and S_7. The equivalent circuits for these operating modes are shown in Figs. 2*a* and *b*.

At $t = T_{\text{ON1}}$, the boost chopper switch S_a is turned ON and the current through inductor L_1 raises linearly from I_1 to I_2. The

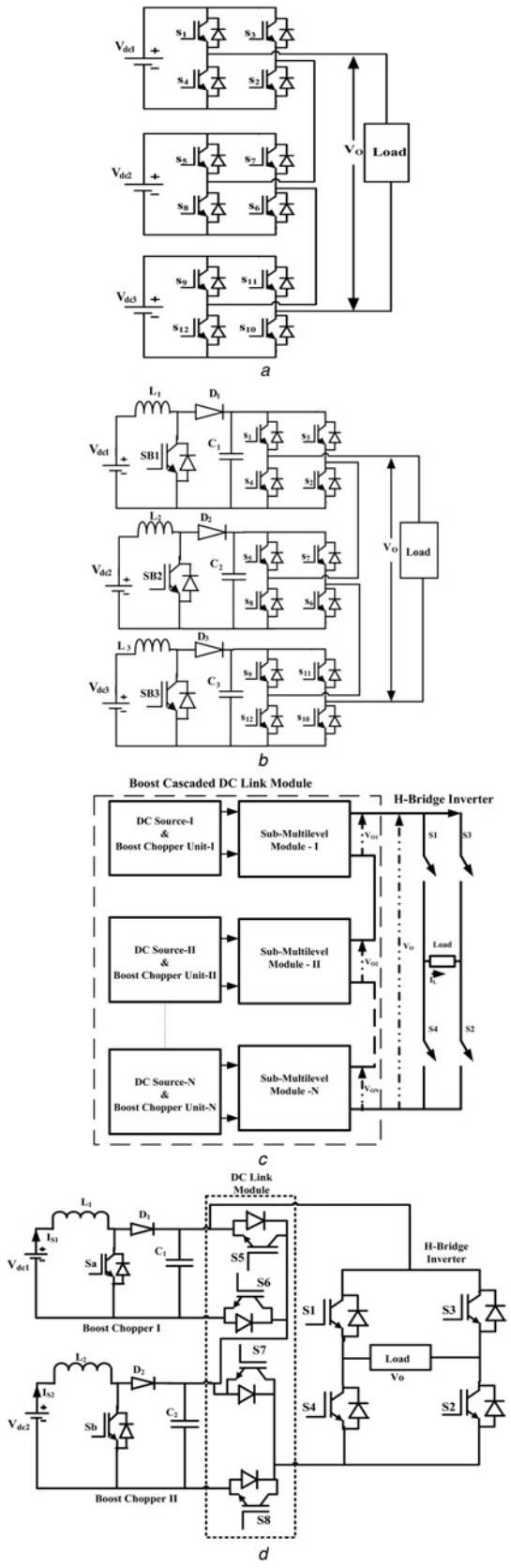

Fig. 1 *Structures*

a Structure of CMLI
b Structure of BCMLI
c Structure of BDCLCMLI
d Equivalent circuit of BDCLCMLI

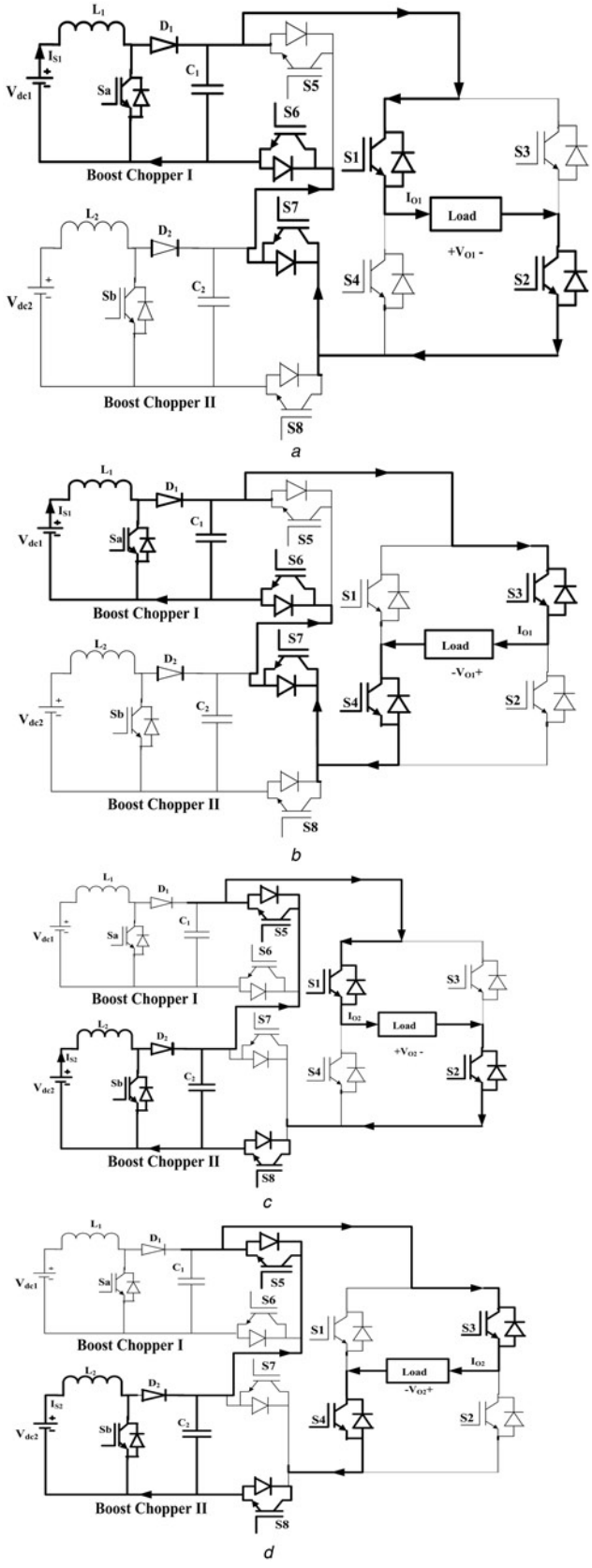

Fig. 2 *Modes of operations of BDCLCMLI*

a Mode 1
b Mode 4
c Mode 2
d Mode 5

IET Power Electron., 2015, Vol. 8, Iss. 11, pp. 2085–2096

voltage across the inductor L_1 is expressed as

$$V_{dc1} = L_1 \frac{I_2 - I_1}{T_{ON1}} \tag{3}$$

At this instant, the energy input to the inductor L_1 from the source V_{dc1} is expressed as

$$E_{i1} = V_{dc1} \cdot I_{s1} \cdot T_{ON1} \tag{4}$$

At $t = T_{OFF1}$, the boost chopper switch S_a is turned OFF and the current through the inductor L_1 falls linearly from I_2 to I_1.

The average output voltage of boost chopper I can be expressed using (5)

$$V_{ob1} = V_{dc1} + L_1 \frac{dI_{s1}}{T_{OFF1}} \tag{5}$$

At this instant, the energy released by the inductor L_1 to the DCLM is given by (6)

$$E_{o1} = (V_{ob1} - V_{dc1}) I_{s1} \cdot T_{OFF1} \tag{6}$$

Considering the system to be lossless, the average output voltage of boost chopper I is obtained using (7)

$$V_{ob1} = \frac{V_{dc1}}{1 - K_1} \tag{7}$$

The change in voltage across the capacitor C_1 can be expressed by (8)

$$\Delta V_{C_1} = I_{o1} * \left[\frac{V_{ob1} - L_1(I_2 - I_1)}{V_{ob1} * f * C_1} \right] \tag{8}$$

where V_{dc1} is the DC source voltage I, I_{s1} is the DC source current I, K_1 is the duty cycle of boost chopper I, V_{ob1} is the output voltage of boost chopper I and f is the switching frequency of boost chopper.

Modes 2 and 5 operations: In modes 2 and 5 operations, the source voltage V_{dc2} is boosted to V_{ob2} by activating the boost chopper switch S_b and the conducting DC-link switches are S_5 and S_8. The respective equivalent circuit for these operating modes is given in Figs. 2*c* and *d*.

At $t = T_{ON2}$, the boost chopper switch S_b is turned ON and the current through the inductor L_2 raises linearly from I_3 to I_4. The voltage across the inductor L_2 is expressed as

$$V_{dc2} = L_2 \frac{I_4 - I_3}{T_{ON2}} \tag{9}$$

At this instant, the energy input to the inductor L_2 from the source can be calculated using (10)

$$E_{i2} = V_{dc2} \cdot I_{s2} \cdot T_{ON2} \tag{10}$$

At $t = T_{OFF2}$, the boost chopper switch S_b is turned OFF and the current through the inductor L_2 falls linearly from I_4 to I_3.

The average output voltage of boost chopper II is obtained using (11)

$$V_{ob2} = V_{dc2} + L_2 \frac{dI_{s2}}{T_{OFF2}} \tag{11}$$

At this instant, the energy released by the inductor L_2 to the DCLM is given by (12)

$$E_{o2} = (V_{ob2} - V_{dc2}) I_{s2} \cdot T_{OFF2} \tag{12}$$

Assuming the system to be lossless, the average output voltage of boost chopper II is obtained using (13)

$$V_{ob2} = \frac{V_{dc2}}{1 - K_2} \tag{13}$$

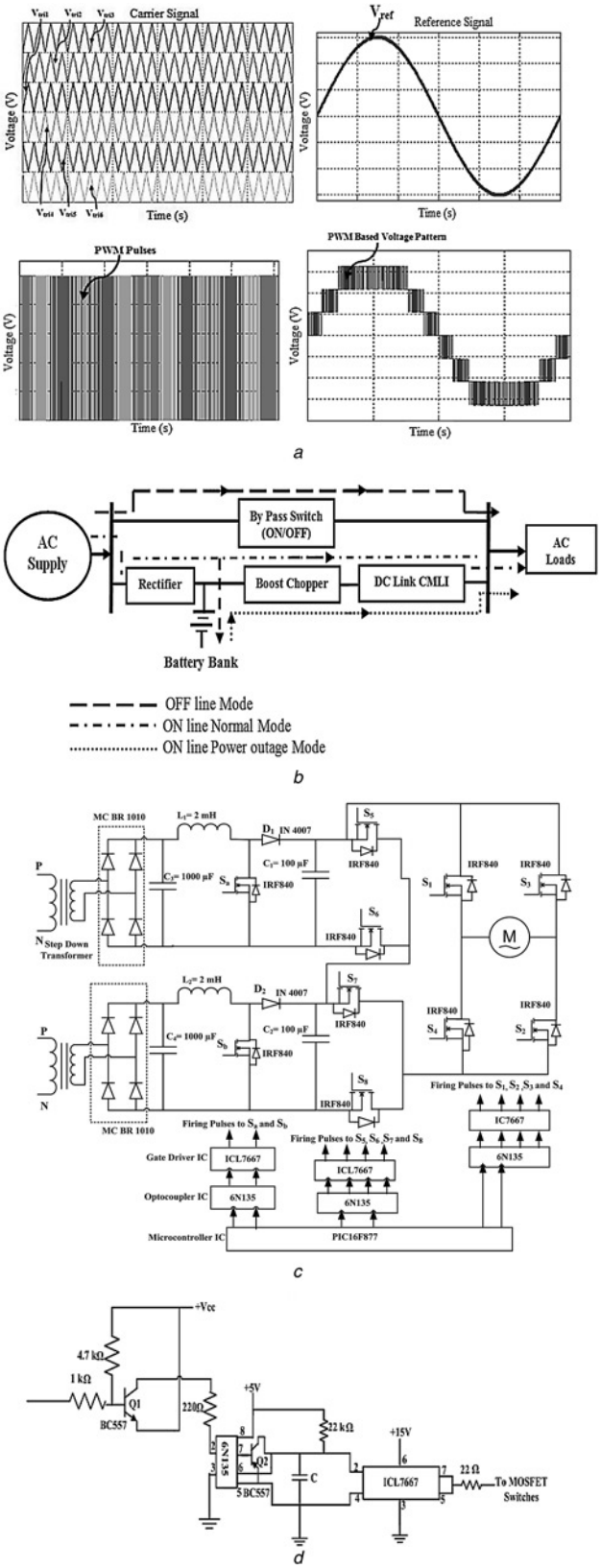

Fig. 3 *Realisation of BDCLCMLI and its switching technique*

a Patterns of carrier signal, reference signal, PWM pulses and output voltage
b Schematic diagram of BDCLCMLI configuration-based UPS system
c Hardware realisation circuit
d Gate driver circuit

Table 1 Switching states of BDCLCMLI

Voltage rating, V	Levels	Switching states									
		S_a	S_b	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
108.4	1	1	0	1	1	0	0	0	1	1	0
216.8	2	0	1	1	1	0	0	1	0	0	1
325.2	3	1	1	1	1	0	0	0	1	0	1
0	4	0	0	0	0	0	0	0	0	0	0
−108.4	5	1	0	0	0	1	1	0	1	1	0
−216.8	6	0	1	0	0	1	1	1	0	0	1
−325.2	7	1	1	0	0	1	1	0	1	0	1

Table 2 Technical specifications of IRF840 MOSFET

Sl. no.	Specifications		Range
1	drain-to-source break down voltage	V_{DS}	500 V, min
2	static drain-to-source on-resistance	R_{DS}	0.85 Ω
3	source current	I_S	8 A
4	gate–source voltage	V_{GS}	±20 V
5	power dissipation	P_D	125 W
6	diode forward voltage	V_{SD}	2 V
7	gate-to-source forward leakage current	I_{GSS}	100 nA
8	gate-to-source reverse leakage current	I_{GSS}	−100 nA
9	drain-to-source leakage current	I_{DSS}	25 μA
10	turn-on delay time	$T_{d\ (on)}$	14 ns

The change in voltage across the capacitor C_2 is expressed by (14)

$$\Delta V_{C_2} = I_{o2}{}^{*}\left[\frac{V_{ob2} - L_2(I_4 - I_3)}{V_{ob2}{}^{*}f{}^{*}C_2}\right] \tag{14}$$

where V_{dc2} is the DC source voltage II, I_{s2} is the DC source current II, K_2 is the duty cycle of boost chopper II and V_{ob2} is the output voltage of boost chopper II.

Modes 3 and 6 operations: In modes 3 and 6 operations, the source voltage V_{dc1} and V_{dc2} are boosted to V_{ob1} and V_{ob2} by activating the boost chopper switches S_a and S_b, respectively, and the conducting DC-link switches are S_6 and S_8.

At $t = T_{ON3}$, the boost chopper switches S_a and S_b are turned ON and the current through the inductors L_1 and L_2 raise linearly from I_1 to I_2 and from I_3 to I_4, respectively.

At this instant, the energy input to the inductor L_1 from the source V_{dc1} and the energy input to the inductor L_2 from the source V_{dc2} are expressed using (15)

$$E_{i3} = (V_{dc1} + V_{dc2}) \cdot (I_{s1} + I_{s2}) \cdot T_{ON3} \tag{15}$$

At $t = T_{OFF3}$, the boost chopper switches S_a and S_b are turned OFF and the current through inductors L_1 and L_2 fall linearly from I_2 to I_1 and from I_4 to I_3, respectively.

At this instant, the energy released from the inductors L_1 and L_2 to the DCLM is given by

$$E_{o3} = \left[(V_{ob1} - V_{dc1})I_{s1} + (V_{ob2} - V_{dc2})I_{s2}\right] \cdot T_{OFF3} \tag{16}$$

The change in voltage across the capacitors C_1 and C_2 is expressed using (17)

$$\Delta V_{C_1} + \Delta V_{C_2} = I_{o1}{}^{*}\left[\frac{V_{o1} - L_1(I_2 - I_1)}{V_{o1}{}^{*}f{}^{*}C_1}\right] + I_{o2}{}^{*}\left[\frac{V_{o2} - L_2(I_4 - I_3)}{V_{o2}{}^{*}f{}^{*}C_2}\right] \tag{17}$$

2.2.2 Operation of H-bridge inverter configuration: H-bridge inverter consists of four controlled power semiconductor switches S_1, S_2, S_3 and S_4. In the conventional inverter system, a constant DC voltage is fed to H-bridge inverter for obtaining AC output. Under this condition, H-bridge inverter switches are subjected to forced commutation. However in the proposed system, the DC-link unidirectional stepped voltage is fed to H-bridge inverter for obtaining AC output. Moreover, inverter switches in each H-bridge are turned ON and turned OFF at zero-voltage magnitudes of DC-link voltage (i.e. H-bridge inverter switches are subjected to zero-voltage switching). Hence, the voltage stress across the inverter switches gets minimised. H-bridge inverter system is operated under two modes of operation. In mode (a) operation, the positive half cycle of AC output voltage is synthesised by activating H-bridge switches S_1 and S_2 as shown in Figs. 2*a* and *c*. The positive half cycle magnitudes of AC output voltage are expressed using (18)–(20)

$$V_{o1} = V_{ob1} \tag{18}$$

$$V_{o2} = V_{ob2} \tag{19}$$

$$V_o = V_{o1} + V_{o2} = V_{ob1} + V_{ob2} \tag{20}$$

In mode (b) operation, the negative half cycle of AC output voltage is synthesised by activating H-bridge switches S_3 and S_4 as shown in Figs. 2*b* and *d*. The negative half cycle magnitudes of AC output voltage are given by

$$V_{o1} = -V_{ob1} \tag{21}$$

$$V_{o2} = -V_{ob2} \tag{22}$$

$$V_o = [V_{o1} + V_{o2}] = -[V_{ob1} + V_{ob2}] \tag{23}$$

3 MCSPWM switching technique

Modulation techniques can be classified according to the switching frequency. Existing modulation techniques such as sinusoidal PWM, space-vector PWM and selective harmonic elimination have been developed to reduce the distortion in MLIs. The MCSPWM control methods are classified as vertical carrier distribution and horizontal carrier distribution [2]. MCSPWM switching pattern is promoted to trigger the DC-link switches of BDCLCMLI.

The output voltage and current harmonics of the proposed system are analysed for different amplitude modulation indices ($M_a = 0.8$, 0.95, 1 and 1.2) and frequency modulation indices ($M_f = 180$, 200 and 220). The proposed system reduced the harmonic content for $M_a = 1$ and $M_f = 200$. For developing the firing pulses of DC-link switches, N_{level}-1 pattern of triangular signals are compared with sinusoidal reference signal. When the magnitude of reference signal (V_{ref}) is greater than triangular signals (V_{tri1}, V_{tri2} and V_{tri3}), the corresponding pulses p_1, p_2 and p_3 are generated as follows

$$p_1 = V_{ref} > V_{tri1} \tag{24}$$

$$p_2 = V_{ref} > V_{tri2} \tag{25}$$

$$p_3 = V_{ref} > V_{tri3} \tag{26}$$

Sub-PWM pulses p_5, p_6, p_7 and p_8 are synthesised from the combination of p_1, p_2 and p_3 pulses which are expressed as follows

IET Power Electron., 2015, Vol. 8, Iss. 11, pp. 2085–2096

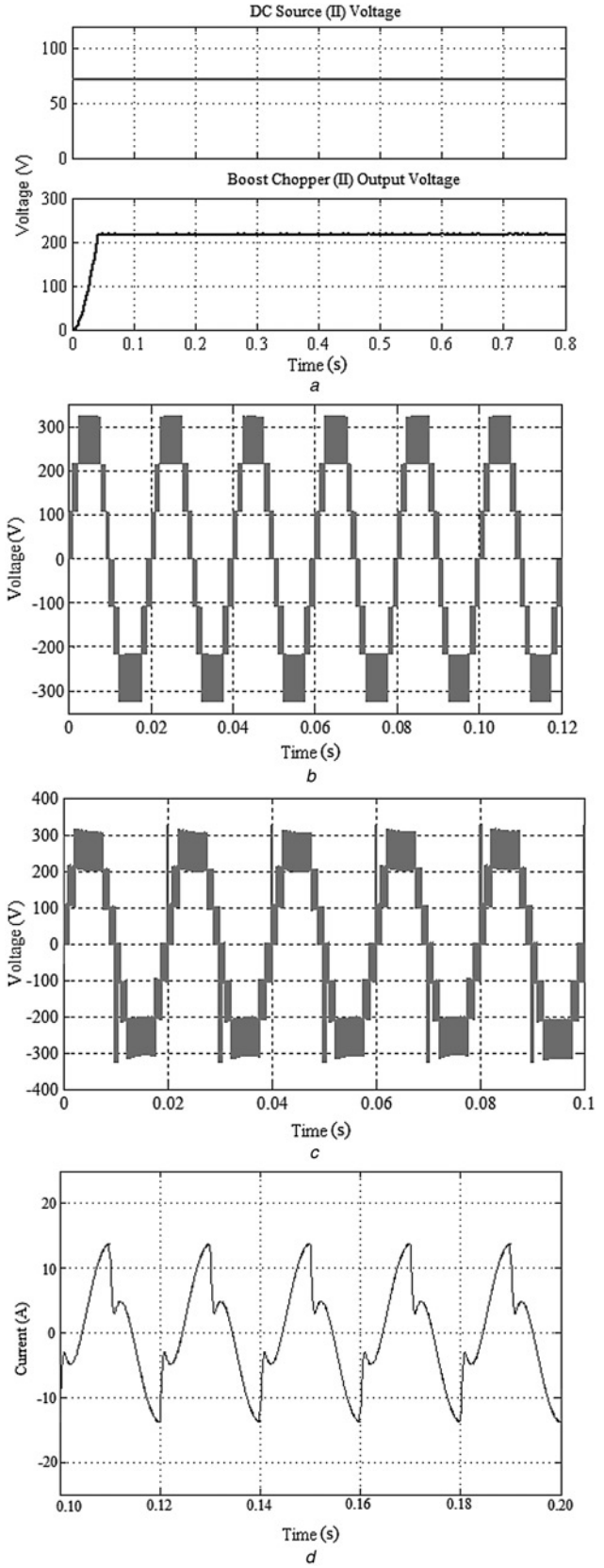

Fig. 4 *Performance evaluation*

a Input and output voltages of boost chopper II (for $M_a = 1$, $M_f = 200$ and $V_{max} = 325$ V)
b UPS (inverter) output voltage for R-load
c UPS (inverter) output voltage for motor drive system
d Drive current

$$p_5 = p_2 \oplus p_3 \tag{27}$$

$$p_6 = p_5 \oplus p_3 \tag{28}$$

$$p_7 = p_1 \oplus p_2 \tag{29}$$

$$p_8 = p_2 \tag{30}$$

When the magnitude of reference signal (V_{ref}) is greater than triangular signals (V_{tri4}, V_{tri5} and V_{tri6}), then the corresponding pulses n_1, n_2 and n_3 are generated. Sub-PWM pulses n_5, n_6, n_7 and n_8 are synthesised from the combination of n_1, n_2 and n_3 pulses. Corresponding sub-PWM pulses are combined to engender the PWM switching pulses for DC-link switches using (31)

$$P_{Si} = p_i + n_i \quad (i = 5,\ 6,\ 7,\ 8) \tag{31}$$

The patterns of carrier signal, reference signal, PWM pulses and the output voltage are shown in Fig. 3*a*. The switching states of BDCLCMLI system are arrayed in Table 1.

4 Realisation of hardware prototype model

4.1 System development

The 1Ø BDCLCMLI-based UPS system configuration is designed and implemented for 150 V (V_{max}) output voltage. The schematic diagram of the proposed system is shown in Fig. 3*b*. The prototype model consists of rectifier units, boost chopper units, controller units, driver units, DC-link and H-bridge inverter units. The rectifier units are designed using bridge rectifier MICBR1010 and a capacitive filter of 1000 µF. The outputs of rectifier units act as the input for the boost chopper units and battery banks. The boost chopper units (Unit I and Unit II) are fabricated using IRF840 power metal–oxide semiconductor field-effect transistor (MOSFET) switches and passive components ($L_1 = L_2 = 2$ mH and $C_1 = C_2 = 100$ µF). The microcontroller (PIC16F877A) provides the control signals to the MOSFET driver circuit. The various features of microcontroller aid to achieve an effective control of the proposed system. The DCLM and H-bridge inverter systems are fabricated using IRF840 power MOSFET switches. The hardware equivalent circuit of BDCLCMLI system is shown in Fig. 3*c*. Driver units consist of ICL7667 integrated circuit (IC) and its biasing components are shown in Fig. 3*d*. Isolation process is achieved by 6N135 IC. The technical specifications of IRF840 power MOSFET are entailed in Table 2.

4.2 Modes of operations

The proposed BDCLCMLI-based UPS system can be operated under three modes: OFF line mode, ON line normal mode and ON line power outage mode. In OFF line mode, the bypass switch activated and the loads are directly connected to the AC utility. In this mode, the battery bank gets charged by the rectified DC supply. In ON line normal mode, the rectifier units convert the AC supply into DC supply. The rectified DC supply is provided both to the battery backup as well as to the load through the proposed system.

The working of the proposed system has already been discussed in Section 2. In ON line power outage mode, the rectifier unit is deactivated. The entire load is operated by battery bank via BDCLCMLI systems. In both the ON line modes, bypass switch is in OFF state. Power flow at various modes is indicated with different dotted lines as shown in Fig. 3*b*. The performance of the UPS system is discussed in Section 5.

4.3 Calculation of losses

The total losses include conduction and switching losses.

4.3.1 Conduction losses: The conduction losses are calculated during on-state of power semiconductor switches. On-state power losses can be calculated from the threshold voltage (V_T) and drain-to-source resistance (R_{DS}) of the power device (MOSFET).

Table 3 Individual harmonic analysis for various amplitude modulation index (for R-load, $V_m = 325$ V)

Harmonic order	$M_a = 0.8$		$M_a = 0.95$		$M_a = 1$		$M_a = 1.2$	
	Voltage harmonics, %	Current harmonics, %	Voltage harmonics, %	Current harmonics, %	Voltage harmonics, %	Current harmonics, %	Voltage harmonics, %	Current harmonics, %
3	0.5	0.5	0.16	0.16	0.17	0.17	6.48	6.48
5	0.37	0.37	0.43	0.43	0.36	0.36	3.13	3.13
7	0.05	0.05	0.18	0.18	0.02	0.02	0.87	0.87
9	0.1	0.1	0.06	0.06	0.02	0.02	0.76	0.76
11	0.03	0.03	0.11	0.11	0.07	0.07	0.64	0.64
13	0.04	0.04	0	0	0.05	0.05	0.03	0.03
15	0.05	0.05	0.02	0.02	0.02	0.02	0.24	0.24
17	0.04	0.04	0.01	0.01	0.04	0.04	0.22	0.22
19	0.06	0.06	0.01	0.01	0.03	0.03	0.02	0.02

Table 4 Individual harmonic analysis for various frequency modulation index (for R-load, $V_m = 325$ V)

Harmonic order	$M_f = 180$		$M_f = 200$		$M_f = 220$	
	Voltage harmonics, %	Current harmonics, %	Voltage harmonics, %	Current harmonics, %	Voltage harmonics, %	Current harmonics, %
3	1.717	1.717	0.17	0.17	1	1
5	0.47	0.47	0.36	0.36	0.44	0.44
7	0.53	0.53	0.02	0.02	0.22	0.22
9	0.51	0.51	0.02	0.02	0.39	0.39
11	0.09	0.09	0.07	0.07	0.05	0.05
13	0.17	0.17	0.05	0.05	0.1	0.1
15	0.09	0.09	0.02	0.02	0.58	0.58
17	0.47	0.47	0.04	0.04	0.66	0.66
19	0.58	0.58	0.03	0.03	0.24	0.24

Table 5 Individual harmonic analysis for various amplitude modulation index (for motor drive, $V_m = 325$ V)

Harmonic order	$M_a = 0.8$		$M_a = 0.95$		$M_a = 1$		$M_a = 1.2$	
	Voltage harmonics, %	Current harmonics, %	Voltage harmonics, %	Current harmonics, %	Voltage harmonics, %	Current harmonics, %	Voltage harmonics, %	Current harmonics, %
3	4.9	8.25	2.57	2.1	2.64	4.25	7.77	17.77
5	7.82	10.9	6.12	10.77	5.62	4.78	4.37	8.68
7	6.09	6.21	5.14	7.77	5.3	3.72	4.85	8.25
9	4.58	5.21	4.76	5.97	4.4	3.62	4.13	5.6
11	3.92	3.68	4.11	4.28	4.12	3.41	3.11	3.5
13	3.43	2.73	3.51	3.11	3.48	3.04	3.54	3.37
15	3.4	2.34	3.02	2.33	3	2.27	3.37	2.78
17	3.7	2.24	2.8	1.9	2.63	1.76	2.55	1.86
19	4.09	2.21	2.73	1.66	2.46	1.48	2.37	1.55

The threshold voltage is a function of junction temperature and the current flowing through the device. The conduction losses of boost chopper switch are calculated using (32)

$$P_B = \sum_{k=1}^{N\text{switch}} V_{T,k} \cdot i_{sw,k} \tag{32}$$

The conduction losses of DCLM switch are expressed by (33), (34)

$$P_{DCLM} = 1/\pi \int_0^{\pi} p_{DCLM}(t)\, d\omega t \tag{33}$$

$$P_{DCLM} = \frac{2I_{01P}}{\pi}(V_{TDCLM}) + \frac{I_{0p}^{\alpha+1}}{(\pi/\omega)} R_{DCLM} \int_0^{\pi} \sin^{\alpha+1}(\omega t)\, dt \tag{34}$$

Table 6 Individual harmonic analysis for various frequency modulation index (for motor drive, $V_m = 325$ V)

Harmonic order	$M_f = 180$		$M_f = 200$		$M_f = 220$	
	Voltage harmonics, %	Current harmonics, %	Voltage harmonics, %	Current harmonics, %	Voltage harmonics, %	Current harmonics, %
3	3.37	6.8	2.64	4.25	2.85	5.27
5	5.15	9.85	5.62	4.78	6.01	11.22
7	4.63	7.37	5.3	3.72	5.66	7.23
9	4.46	5.85	4.4	3.62	4.48	5.76
11	3.92	4.25	4.12	3.41	4.41	4.68
13	3.14	2.91	3.48	3.04	4.14	3.21
15	2.82	2.27	3	2.27	3.57	2.73
17	2.82	2.23	2.63	1.76	3.22	2.55
19	2.71	2.17	2.46	1.48	3.35	2.46

IET Power Electron., 2015, Vol. 8, Iss. 11, pp. 2085–2096

The conduction losses of H-bridge inverter switch are calculated using (35)

$$P_{\mathrm{H}} = 1/\pi \int_0^{\pi} p_h(t)\,\mathrm{d}\omega t \tag{35}$$

The total conduction losses of the proposed system are given by

$$P_{\mathrm{BDCLCMLI}} = P_B + P_{\mathrm{DCLM}} + P_H \tag{36}$$

where I_{0P} is the maximum load current and α is a constant.

4.3.2 Switching losses: The switching losses during the turn ON and OFF conditions of boost chopper switch are calculated using (37), (38)

$$E_{\mathrm{on},B} = \sum_{k=1}^{N_{\mathrm{switch}}} V_{\mathrm{sw},k} \cdot i_{\mathrm{sw},k} \cdot t_{\mathrm{on}} \tag{37}$$

$$E_{\mathrm{off},B} = \sum_{k=1}^{N_{\mathrm{switch}}} V_{\mathrm{sw},k} . i'_{\mathrm{sw},k} \cdot t_{\mathrm{off}} \tag{38}$$

The switching losses during the turn ON and OFF conditions of DCLM switch are expressed using (39)–(42)

$$E_{\mathrm{on},K} = (V_{\mathrm{sw},k} \cdot i_{\mathrm{sw},k} \cdot t_{\mathrm{on}})/6 \tag{39}$$

$$E_{\mathrm{on,DCLM}} = \sum_{k=1}^{N_{\mathrm{switch}}} E_{\mathrm{on},K} \tag{40}$$

$$E_{\mathrm{off},k} = (V_{\mathrm{sw},k} \cdot i'_{\mathrm{sw},k} \cdot t_{\mathrm{off}})/6 \tag{41}$$

$$E_{\mathrm{off,DCLM}} = \sum_{k=1}^{N_{\mathrm{switch}}} E_{\mathrm{off},K} \tag{42}$$

where $E_{\mathrm{on}\text{-}k}$ is the turn-on loss of the switch k, $E_{\mathrm{off}\text{-}k}$ is the turn-off loss of the switch k, i_{sw} is the current flowing through the switch after turning ON and i'_{sw} is the current flowing through the switch before turning ON.

International rectifier (IR) made of MOSFET IRF840 switches is used for the hardware implementation of conventional seven-level CMLI configuration. By the data provided by IR, the voltage drop and the on-state resistance are considered to be 2.5 V and 0.85 Ω, respectively. About 12 switches are required to obtain the staircase AC output voltage of conventional seven-level CMLI as depicted in Table 10. As per IR data consideration, the on-state power loss of each MOSFET switch is calculated as 7.35 W. The on-state power loss of conventional seven-level CMLI configuration is obtained as 44.1 W (for obtaining the positive half cycle). If the boost chopper configuration is provided in the front end of each H-bridge of conventional seven-level CMLI, three more MOSFET switches are getting added with CMLI topology. Hence, the on-state power loss of seven-level boost CMLI topology is obtained as 66.15 W.

Totally eight MOSFET switches are utilised to obtain the staircase AC output voltage of seven-level DCLCMLI configuration. As per IR data consideration, the on-state power loss of seven-level DCLCMLI configuration is obtained as 29.4 W (for obtaining the positive half cycle). For the proposed BDCLCMLI configuration, only two MOSFET switches are getting added with DCLCMLI topology. Hence, the on-state power loss of seven-level boost CMLI topology is calculated as 44.1 W.

From the above analysis, it is inferred that the proposed BDCLCMLI configuration reduces the on-state power loss to 29.17% compared with that of conventional boost CMLI topology. Since, the staircase AC output voltages of both the conventional and the proposed configurations are symmetrical in nature, the on-state power loss for obtaining the negative half cycle can be considered as same as that of positive half cycle.

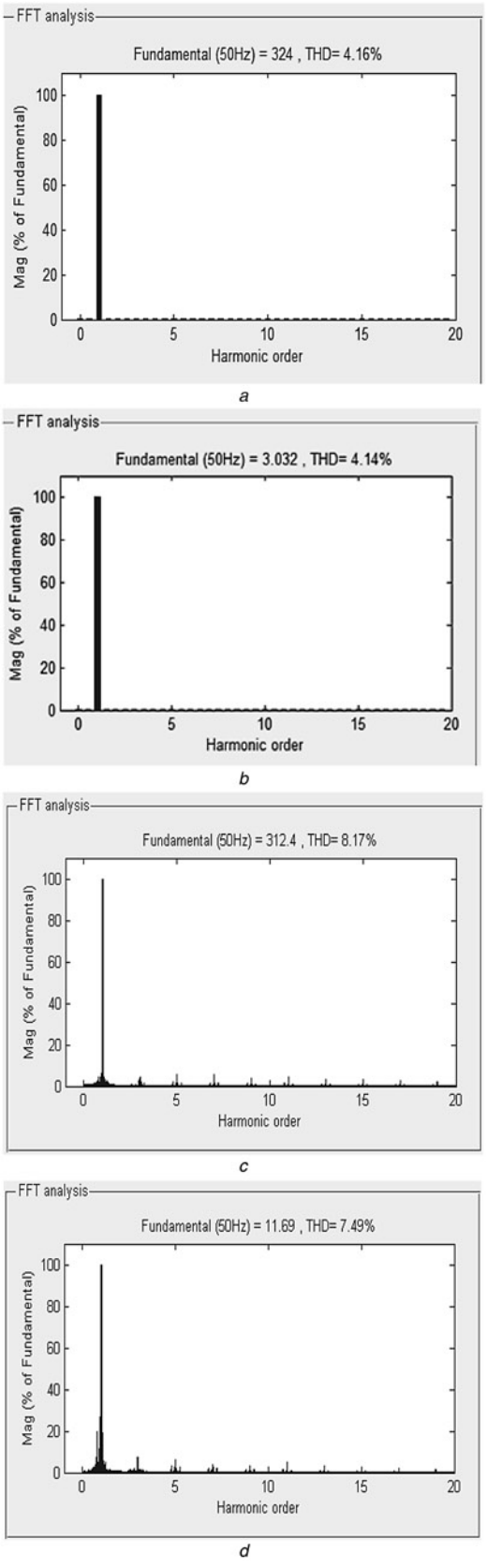

Fig. 5 *Voltage and current THD spectrum (for $M_a = 1$ and $M_f = 200$)*

a, *b* For resistive load system
c, *d* For motor drive system

4.4 Design of boost chopper parameters

The system parameters are designed for the inverter output voltage of 150 V (V_m).

From (7) the average output voltage of boost chopper I is

$$V_{ob1} = 36.3/(1 - 0.31) \quad \text{(assuming } K_1 = 0.31\text{)}$$
$$V_{ob1} = 52.6\,\text{V}$$

From (8) and (14) the values of L_1 and L_2 are calculated using (43), (44)

$$L_1 = \frac{V_{dc1}{}^*(V_{ob1} - V_{dc1})}{(I_2 - I_1)^* f^* V_{ob1}} \tag{43}$$

$$L_2 = \frac{V_{dc2}{}^*(V_{ob2} - V_{dc2})}{(I_4 - I_3)^* f^* V_{ob2}} \tag{44}$$

The value of inductor L_1 can be obtained by suitably substituting the parametric values in (43) and it is found that $L_1 = 2$ mH.

4.5 Cost analysis

To reduce the voltage stress on the two-level and three-level inverters, an auxiliary resonant circuit is introduced in the DC-link systems [25]. To achieve boost operation in the conventional two-level systems, magnetic component such as transformer is required at the rectifier side. Moreover, to obtain sinusoidal output voltage, expensive LC filter is required at the inverter end. The usage of transformers, filter and resonant soft switching circuits such as power switches, inductors and capacitors in two-level and three-level inverters leads to high cost. To achieve minimal harmonic distortion at the output voltage of the seven-level CMLI [5–8], additional DC sources, power semiconductor devices and controller units are required. The requirement of power devices and DC sources for various systems are analysed in Tables 10 and 11. From the analysis, it is observed that the proposed system requires minimal DC sources and power switches. Obviously, it reduces the overall cost of the proposed system.

Owing to the emerging trends in the development of power semiconductor devices, the proposed system can be implemented for achieving the smooth control of variable speed AC drives, utility interface, active power filtering, unified power flow controllers and static compensator (STATCOM) applications.

5 Performance analysis

The simulation is carried out and analysed using MATLAB for the AC output voltage conditions of 325 V (V_{max}) and 150 V (V_{max}), respectively. The experimental results are validated for the AC output voltage 150 V (V_{max}).

5.1 Performance evaluation (for $V_m = 325$ V)

The DC source (battery bank) voltage V_{dc1} of 36 V is boosted to 110 V and another DC source (battery bank) voltage V_{dc2} of 72 V is boosted to 215 V as shown in Fig. 4*a*. Figs. 4*b* and *c*, respectively, show the UPS (inverter) output voltage ($V_m = 325$ V) waveforms of the proposed BDCLCMLI fed R-load and motor drive systems. The induction motor drive current ($I_m = 11.69$ A) of the proposed system is shown in Fig. 4*d*. Voltage spike is observed in the output voltage of DCLM and H-bridge inverter of BDCLCMLI fed motor drive system as shown in Figs. 4*c*, 8*a* and *c*, respectively. Certain investigations have been made using MATLAB and it is understood that the voltage spike is because of the inductance effect of motor drive system. The voltage spike is not present in the output voltage of BDCLCMLI fed R-load system.

The individual voltage and current harmonic content in the output of BDCLCMLI fed R-load and motor drive analysed for various M_a and M_f are tabulated in Tables 3–6, respectively. Moreover, it is observed that the output voltage and current of the proposed system have lower third-order harmonics and it is found to increase in harmonics level of output voltage and current for raise in M_a. Output voltage and current total harmonic distortion (THD) spectrum of BDCLCMLI fed R-load and motor drive systems are shown in Fig. 5. From the spectrum shown in Figs. 5*a* and *b*, it is viewed that the output voltage and current have almost the same

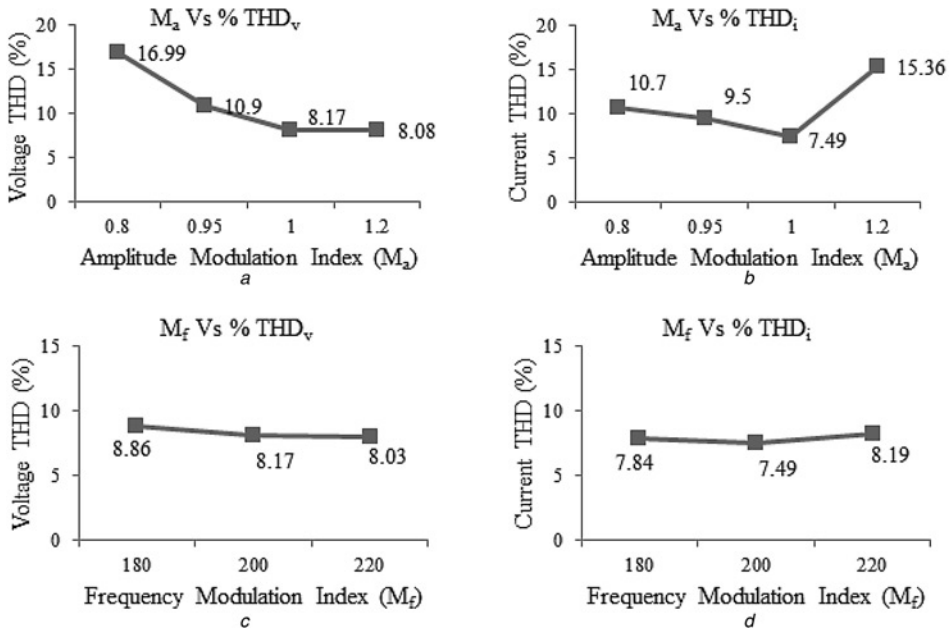

Fig. 6 *Voltage and current THD analysis (for motor drive system, $V_m = 325$ V)*

a M_a against percentage of voltage THD
b M_a against percentage of current THD
c M_f against percentage of voltage THD
d M_f against percentage of current THD

IET Power Electron., 2015, Vol. 8, Iss. 11, pp. 2085–2096

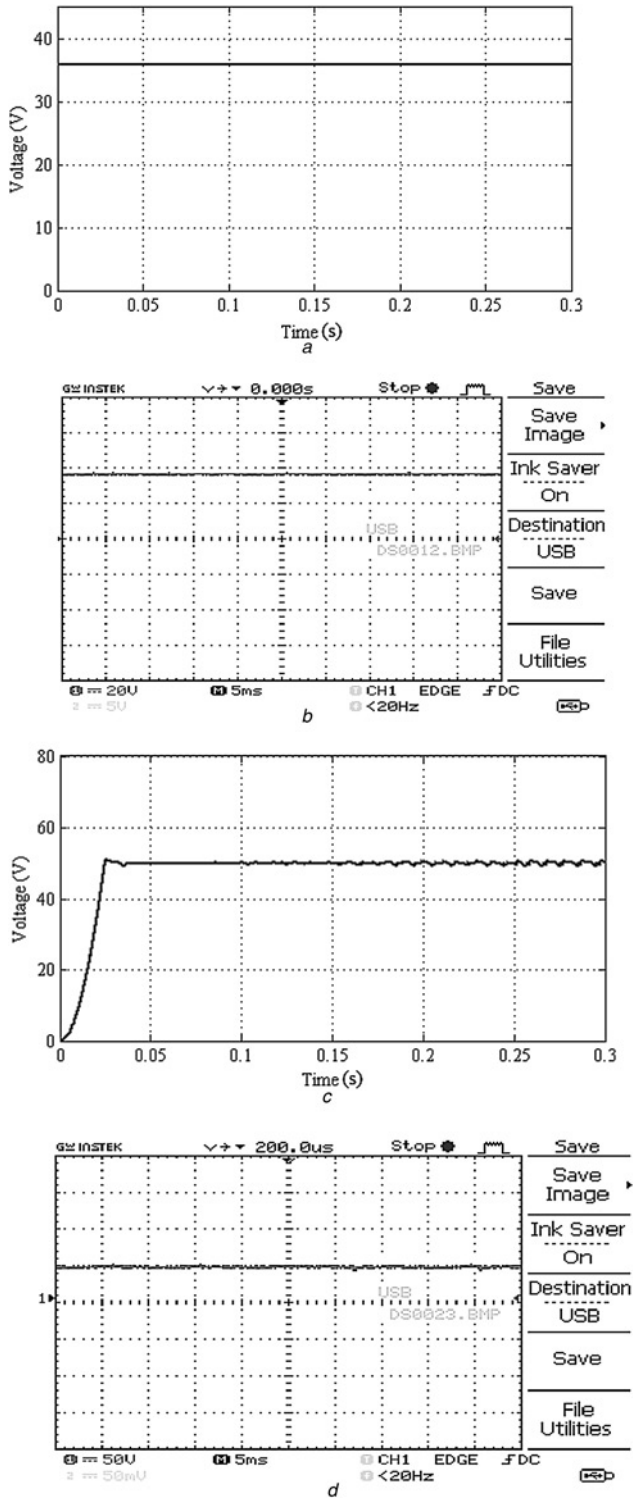

Fig. 7 *Input and Output Voltage of Boost Chopper I*

a Simulated input voltage of boost chopper I
b Experimented input voltage of boost chopper I
c Simulated output voltage of boost chopper I
d Experimented output voltage of boost chopper I

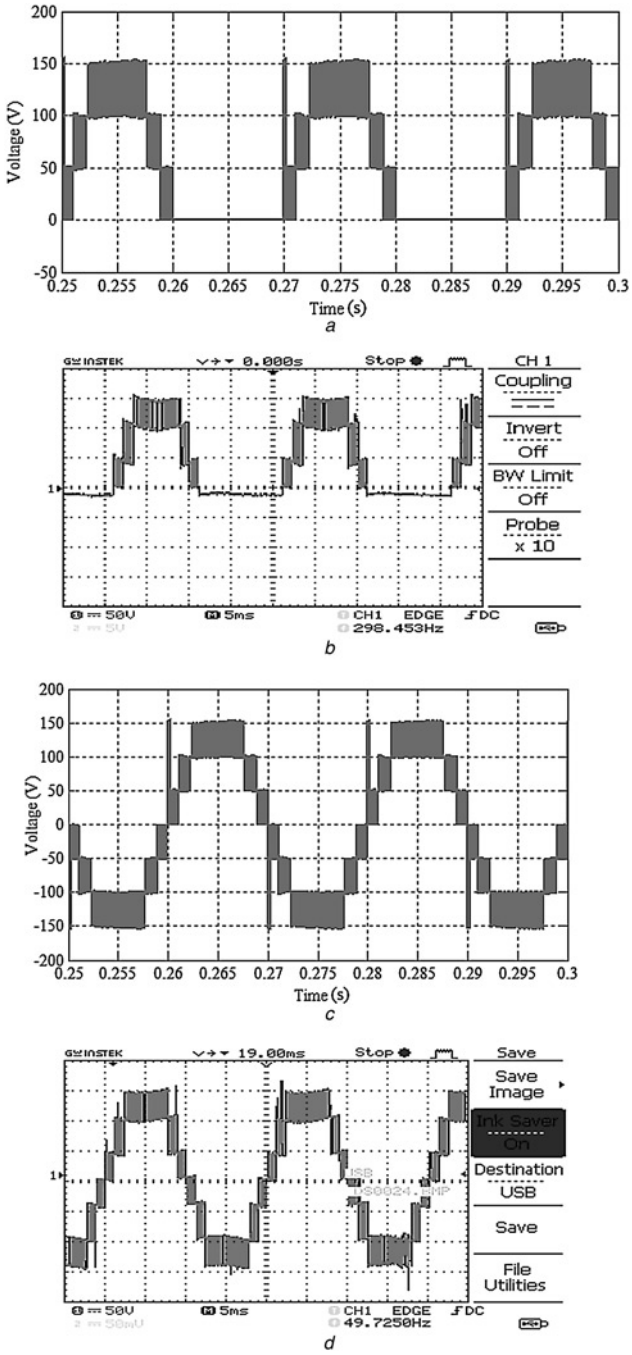

Fig. 8 *Voltage across the H-bridge inverter switches S_3, S_4 and load*

a Simulated voltage across the H-bridge switches S_3 and S_4
b Experimented voltage across the H-bridge switches S_3 and S_4
c Simulated UPS (inverter) output voltage (for $M_a = 1$ and $M_f = 200$)
d Experimented UPS (inverter) output voltage (for $M_a = 1$ and $M_f = 200$)

THD of 4.1%. From the spectrum shown in Figs. 5*c* and *d*, it is viewed that the output voltage and current have the THD of 8.17 and 7.49%, respectively. Output voltage ($V_m = 325$ V) and current THD for various M_a and M_f values are analysed and depicted graphically in Fig. 6. From the detailed harmonic analysis with an output voltage of 325 V, it is inferred that the minimum and acceptable current THD is achieved for $M_a = 1$ and $M_f = 200$.

5.2 Performance evaluation (for $V_m = 150$ V)

The DC source (battery bank) voltages $V_{dc1} = 36$ V and $V_{dc2} = 76$ V are boosted to 50 and 100 V, respectively, by boost chopper units I and II. The source voltage V_{dc1} is obtained from the rectifier unit and illustrated in Figs. 7*a* and *b*. The output voltage of boost chopper I with a magnitude of 50 V obtained is depicted in Figs. 7*c* and *d*. Initially, inverter switches S_1 and S_2 are triggered at 0 ms and the switches S_3 and S_4 are triggered at 10 ms. Voltage across the H-bridge inverter is equal to the DC-link output voltage. The voltage across the H-bridge inverter switches S_3 and S_4 as shown in Figs. 8*a* and *b* is triggered at zero-voltage magnitudes of

Table 7 Individual harmonic analysis for various amplitude modulation index (for motor drive, $V_m = 150$ V)

Harmonic order	$M_a = 0.8$		$M_a = 0.95$		$M_a = 1$		$M_a = 1.2$	
	Voltage harmonics, %	Current harmonics, %	Voltage harmonics, %	Current harmonics, %	Voltage harmonics, %	Current harmonics, %	Voltage harmonics, %	Current harmonics, %
3	4.63	3.62	4.19	3.42	4.01	3.7	9.17	13.83
5	4.91	4.23	5.08	4.67	5.65	4.73	5.22	6.62
7	4.57	3.67	4.35	3.7	4.84	3.72	5.16	5.86
9	4.24	2.5	4.13	3.85	4.51	3.65	4.63	4.3
11	4.08	1.99	3.85	2.46	4.21	2.92	3.8	2.93
13	3.93	1.63	3.59	1.95	3.73	2.25	4.06	2.67
15	3.85	1.39	3.37	1.58	3.41	1.78	3.97	2.26
17	3.76	1.2	3.28	1.36	3.22	1.48	3.32	1.67
19	3.76	1.09	3.22	1.19	3.16	1.3	3.22	1.45

Table 8 Individual harmonic analysis for various frequency modulation index (for motor drive, $V_m = 150$ V)

Harmonic order	$M_f = 180$		$M_f = 200$		$M_f = 220$	
	Voltage harmonics, %	Current Harmonics, %	Voltage harmonics, %	Current harmonics, %	Voltage harmonics, %	Current harmonics, %
3	5	4.66	4.01	3.7	4.23	3.88
5	5.47	4.29	5.65	4.73	5.55	4.92
7	4.34	3.73	4.84	3.72	5.32	4.54
9	4.47	3.29	4.51	3.65	4.81	3.88
11	4.23	2.79	4.21	2.92	4.33	3.74
13	3.85	2.39	3.73	2.25	3.99	2.38
15	3.75	2.17	3.41	1.78	3.47	2.04
17	3.92	2.08	3.22	1.48	3.37	1.89
19	3.95	1.97	3.16	1.3	3.42	1.81

DC-link output voltage. Hence, the voltage stress across the switches is reduced.

Both the simulated and experimental output voltage waveforms of the proposed BDCLCMLI system are shown in Figs. 8*c* and *d*, respectively. Tables 7 and 8 entail the individual voltage and current harmonic content in the 150 V output voltage of BDCLCMLI fed drive system for various M_a and M_f, respectively.

Output voltage and current THD for various M_a and M_f are simulated and presented in Fig. 9. From the analysis of 150 V output voltage system, it is inferred that the minimum current THD is achieved for $M_a = 1$ and $M_f = 200$. The output voltage and current THD of the proposed system for 150 V are shown in Figs. 10*a* and *b*, respectively. From the spectral analysis, it is observed that the voltage and current THD of the proposed

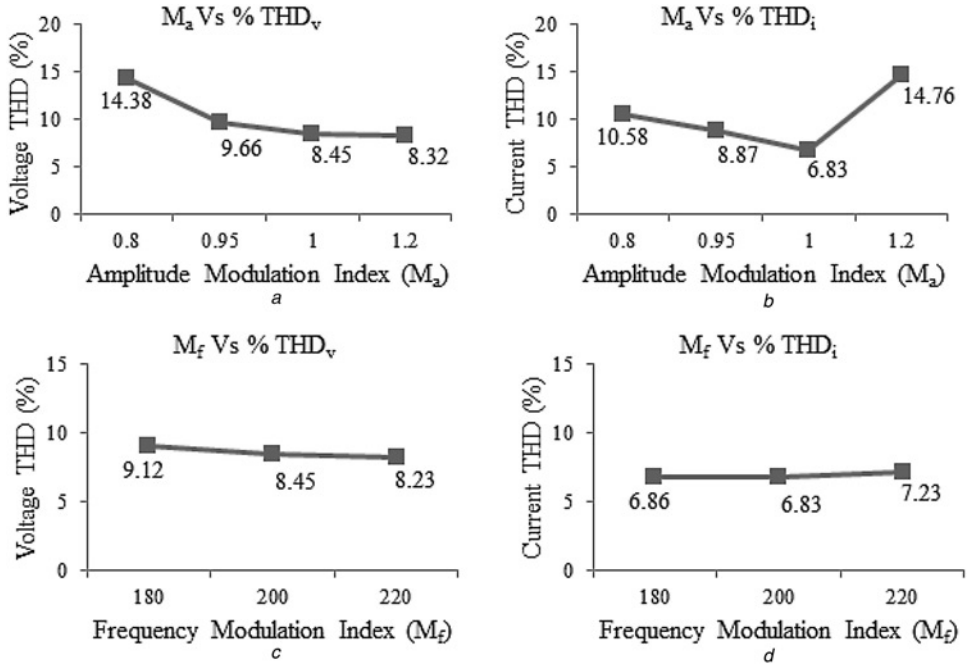

Fig. 9 *Voltage and current THD analysis (for motor drive system, $V_m = 150$ V)*

a M_a against percentage of voltage THD
b M_a against percentage of current THD
c M_f against percentage of voltage THD
d M_f against percentage of current THD

IET Power Electron., 2015, Vol. 8, Iss. 11, pp. 2085–2096

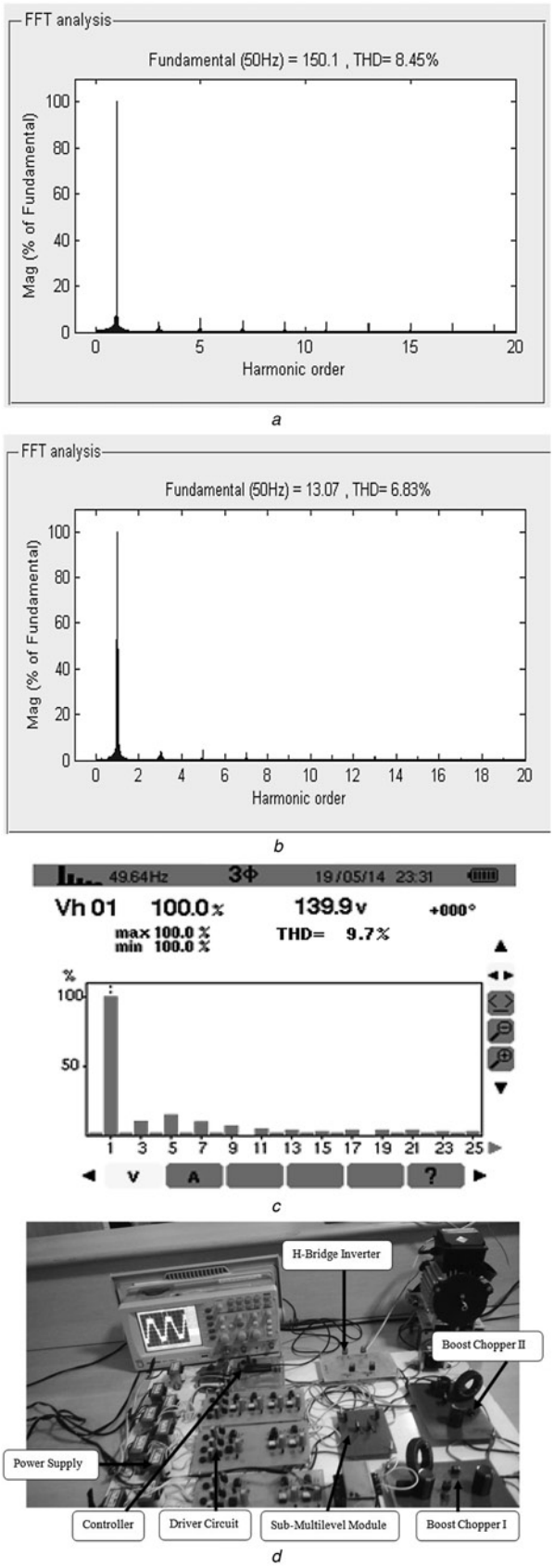

Fig. 10 *Simulated THD spectrum of BDCLCMLI fed AC drive (for 150 V AC output voltage, $M_a = 1$ and $M_f = 200$)*

a Voltage THD
b Current THD
c Experimented voltage THD spectrum of BDCLCMLI
d Experimental setup

Table 9 Specifications of induction motor drive

Sl. no.	Parameters	Range
1	supply voltage, V	220
2	drive current, A	1.2
3	rotor speed, RPM	1430
4	rated power, kW	0.18

Table 10 Power switch count analysis

Levels	Number of controlled switches (MOSFET)		
	CMLI	BCMLI	BDCLCMLI
5	8	10	7
7	12	15	10
15	28	35	13
31	60	75	16

Table 11 DC source count analysis

Levels	Number of DC sources		
	CMLI	BCMLI	BDCLCMLI
5	2	2	1
7	3	3	2
15	7	7	3
31	15	15	4

BDCLCMLI fed 150 V drive system are 8.45 and 6.83%, respectively. Harmonic analysis for the prototype system with an output voltage of 150 V using analyser model name (ALM) ten power quality (PQ) analyser is carried out and the results are presented in Fig. 10*c*. It is observed from the spectral analysis that the inverter output frequency is 49.64 Hz and THD of output voltage is 9.7%. These values almost validate with the simulation results obtained in Fig. 10*a*. The experimental setup of the proposed system is shown in Fig. 10*d*. The technical specifications of single-phase induction motor drive are entailed in Table 9.

5.3 Analysis of DC source and power switch count

The required power switches and DC sources for various systems are analysed and tabulated in Tables 10 and 11, respectively. From the analysis, it is inferred that the proposed BDCLCMLI system required less number of DC sources and power switches than other conventional systems. This proves the economy of the proposed system as detailed in Section 4.5.

6 Conclusion

In this paper, a new structure of seven-level BDCLCMLI has been proposed. The proposed topology extends the design flexibility and the possibility to optimise the power converter for achieving the main objectives. Compared with conventional inverter systems, the proposed system is employed with reduced voltage stress, reduced switch count and DC source count. The proposed BDCLCMLI configuration required at least two DC sources for synthesising seven-level AC output, which is the main constraint of the proposed system. Several analyses in terms of cost, semiconductor loss and harmonics have been made and it is inferred that the proposed structure can be an appropriate aspirant for power converters used in UPS and drive applications.

7 References

1 Lai, J.S., Peng, F.Z.: 'Multilevel converters – a new breed of power converters', *IEEE Trans. Ind. Appl.*, 1996, **5/6**, (32), pp. 509–517
2 Colak, I., Kabalci, E., Bayindir, R.: 'Review of multilevel voltage source inverter topologies and control schemes', *Int. J. Energy Convers. Manage.*, 2010, **9**, pp. 1–15
3 Kouro, S., Malinowski, M., Gopakumar, K., *et al*.: 'Recent advances and industrial applications of multilevel converters', *IEEE Trans. Ind. Electron.*, 2010, **8**, (57), pp. 2553–2580
4 Rodriguez, J., Lai, J.-S., Peng, F.Z.: 'Multilevel inverters: a survey of topologies, controls, and applications', *IEEE Trans. Ind. Electron.*, 2002, **8**, (49), pp. 724–738
5 Liu, Y., Hong, H., Huang, A.Q.: 'Real-time algorithm for minimizing THD in multilevel inverters with unequal or varying voltage steps under staircase modulation', *IEEE Trans. Ind. Electron.*, 2009, **6**, (56), pp. 2249–2258
6 Shen, M., Peng, F.Z., Tolbert, L.M.: 'Multilevel DC–DC power conversion system with multiple DC sources', *IEEE Trans. Power Electron.*, 2008, **1**, (23), pp. 420–426
7 Rahim, N.A., Selvaraj, J.: 'Multistring five-level inverter with novel PWM control scheme for PV application', *IEEE Trans. Ind. Electron.*, 2010, **6**, (57), pp. 2111–2123
8 Uthirasamy, R., Ragupathy, U.S., Kumar Chinnaiyan, V., Megha, C.: 'Experimentation of boost chopper interfaced cascaded multilevel inverter topology for photo voltaic applications', *Int. Rev. Electr. Eng.*, 2014, **1/2**, (9), pp. 16–25
9 Babaei, E.: 'A cascade multilevel converter topology with reduced number of switches', *IEEE Trans. Power Electron.*, 2008, **11**, (23), pp. 2657–2664
10 Ajami, A., Oskuee, M.R.J., Khosroshahi, M.T., Mokhberdoran, A.: 'Cascade-multi-cell multilevel converter with reduced number of switches', *IET Power Electron.*, 2014, **3**, (3), pp. 552–558
11 Miranbeigi, M., Iman-Eini, H., Asoodar, M.: 'A new switching strategy for transformer-less back-to-back cascaded H-bridge multilevel converter', *IET Power Electron.*, 2014, **7**, (7), pp. 1868–1877
12 Masaoud, A., Ping, H.W., Mekhilef, S., Taallah, A.: 'Novel configuration for multilevel DC-link three-phase five-level inverter', *IET Power Electron.*, 2014, **12**, (12), pp. 3052–3061
13 Alishah, R.S., Nazarpour, D., Hosseini, S.H., Sabahi, M.: 'New hybrid structure for multilevel inverter with fewer number of components for high-voltage levels', *IET Power Electron.*, 2014, **1**, (1), pp. 96–104
14 Rodriguez, J., Moran, L., Correa, P., Silva, C.: 'A vector control technique for medium-voltage multilevel inverters', *IEEE Trans. Ind. Electron.*, 2002, **8**, (49), pp. 882–888
15 Corzine, K.A., Wielebski, M.W., Peng, F.Z., Wang, J.: 'Control of cascaded multilevel inverters', *IEEE Trans. Power Electron.*, 2004, **5**, (19), pp. 732–738
16 Odeh, C.I., Agu, V.N., Goshwe, N.: 'Cascaded three-phase pulse-width modulated switched voltage source inverter', *IET Power Electron.*, 2014, **7**, (7), pp. 1925–1983
17 Carrara, G., Gardella, S., Marchesoni, M., Salutari, R., Sciutto, G.: 'A new multilevel PWM method: a theoretical analysis', *IEEE Trans. Power Electron.*, 1992, **7**, (7), pp. 497–505
18 Tolbert, L.M., Habetler, T.G.: 'Novel multilevel inverter carrier-based PWM method', *IEEE Trans. Ind. Appl.*, 1999, **9/10**, (35), pp. 1098–1107
19 McGrath, B.P., Holmes, D.G.: 'Multicarrier PWM strategies for multilevel inverters', *IEEE Trans. Ind. Electron.*, 2002, **8**, (49), pp. 858–867
20 Aneesh Mohamed, A.S., Gopinath, A., Baiju, M.R.: 'A simple space vector PWM generation scheme for any general n-level inverter', *IEEE Trans. Ind. Electron.*, 2009, **5**, (56), pp. 1649–1656
21 Kouro, S., Rebolledo, J., Rodriguez, J.: 'Reduced switching frequency modulation algorithm for high-power multilevel inverters', *IEEE Trans. Ind. Appl.*, 2007, **10**, (54), pp. 2894–2901
22 Leon, J.I., Vazquez, S., Kouro, S., Franquelo, L.G., Carrasco, J.M., Rodriguez, J.: 'Unidimensional modulation technique for cascaded multilevel converters', *IEEE Trans. Ind. Electron.*, 2009, **8**, (56), pp. 2981–2986
23 Yao, W., Hu, H., Lu, Z.: 'Comparisons of space-vector modulation and carrier-based modulation of multilevel inverter', *IEEE Trans. Power Electron.*, 2008, **1**, (23), pp. 45–51
24 Lu, Z.-G., Zhao, L.-L., Zhu, W.-P., Wu, C.-J., Qin, Y.-S.: 'Research on cascaded three-phase-bridge multilevel converter based on CPS-PWM', *IET Power Electron.*, 2013, **7**, (6), pp. 1088–1099
25 Jie, J.H.: 'Modular design of soft-switching circuits for two level and three-level inverters', *IEEE Trans. Power Electron.*, 2006, **1**, (21), pp. 131–139