An Experimental Investigation on Implementation of Advanced Cascaded Multilevel Inverter for Renewable Energy Applications

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Abstract – The investigate on multilevel inverter in these days for various applications goes on hastily due to its efficient process. The scheme proposes an advanced cascaded multilevel inverter which varies from the predictable one from the number of input dc sources used. The planned nine level multilevel inverter configurations utilize a single dc source whereas in the conventional one it varies based on the number of levels. The single phase transformer is replaced by the three phase linear transformer to reduce the number of transformer. The circuit simulation is mode using MATLAB/Simulink software and the performance analysis is made based on the factors like THD, efficiency, cost effectiveness, etc. Also, the hardware results shwos the effectiveness of the ACMLI (Advanced Cascaded Multilevel Inverter) for renewable energy applications like solar water pumping, street lighting,etc.

Keywords--Cascaded multilevel inverter, harmonics, switchingPhase angle control, three-phase transformers.

I. INTRODUCTION

Numerous industrial applications have started utilizing high power applications in recent years. Some medium voltage motor drives and utility applications require medium voltage and mega watt power level for a medium voltage grid; it is troublesome to connect directly a single switch. As a result, multilevel power converter (both rectifiers and inverters), has been introduced as an alternative in high power and medium voltage situations[1],[3]. The concept of multilevel inverters has been introduced since 1975. A multilevel inverter not only archives high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photo voltaic, wind and fuel cells can be easily interfaced to a multilevel inverter (converter) system for a high power application. The multilevel power converters can be referred as voltage synthesizers in which high output voltage is synthesized from many discrete smaller voltages levels. The advantage of multilevel converters when compared to other converters can be listed as follows: they can generate output voltages with extremely low distortion and lower (dv/dt), they draw input current with very low distortion, they can operate with a lower switching frequency, their efficiency is high (>98%) because of the minimum switching frequency, they are suitable for medium to high power applications, multilevel waveform naturally limits the problem of large voltage transients. The selection of the best multilevel topology for each application is often not clear and is subject to various engineering tradeoffs. Among the various MLI's like Diode-clamped multilevel inverter, Capacitor-clamped multilevel inverter and Cascaded multilevel inverter, CMLI is the most commonly used which is more advantageous than other MLIs [2],[3].

II. TYPES OF MULTILEVEL INVERTERS

A. Diode Clamped Multilevel Inverter

The first practical multilevel topology is the neutral point clamped PWM technology first introduced by Nabe, et al, in 1980. For m-level inverter, dc bus voltage is splits into 'm' levels by (m-1) series connected bulk capacitors. Here, diodes clamp the switch voltage to half the level of the dc bus voltage, which is an added

advantage of this type. The advantages of the diode clamped multilevel inverter topology are: When the number of levels is high enough, the harmonic content is low enough to avoid the need for filters, inverter efficiency is high [1],[3]. The disadvantages of the diode clamped multilevel inverter topology are: excessive clamping diodes are required when levels are high, the issue of maintaining the charge balance of the capacitors is still an open issue for NPC topologies with more than three levels.

B. Flying Capacitor Multilevel Inverter

This topology was first proposed in 1992 and is considered to be the serious alternative to the diode clamped topology. In addition to improving the waveform quality, these multilevel inverters substantially reduce voltage stress on the devices. However in this type of inverters the required voltage blocking capabilities of the clamping diodes at higher levels is high [9]. So an alternative multilevel structure where the voltage across an open switch is constrained by clamping diodes has been proposed by Meynard. These inverters are commonly known as flying capacitor. This makes the topology attractive even for the dc/dc conversion. At the present time it seems that this topology has few advantages like: Large amount of storage capacitors can provide capabilities during power outages, Like diode clamped inverters, when the number of levels is high enough, the harmonic content is low enough to avoid the need for filters [3].Both real and reactive power flow can be controlled. Some of the disadvantages of flying capacitor topology are: Excessive number of storage capacitors is required, the inverter control can be very complicated.

C. Cascaded Multilevel Inverter

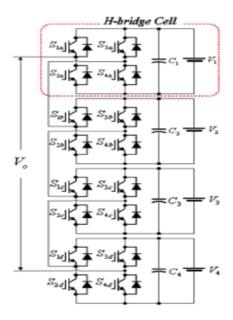


Fig.1. CMLI with independent DC source

An Cascaded Multilevel Inverter with single independent DC sources for each legs is shown in Fig.1., which has 4 legs with 9 levels. This topology employs a cascade of low voltage H-bridges each with independent and isolated dc sources. The phase output voltage is synthesized by the sum of series of H-bridges plus one. One major advantage of this approach is that the number of the output can be further increased without addition of any new components. The advantages of the cascaded multilevel H-bridge converter are the following: scalable, modularized circuit layout and ease of packaging, no extra clamping diodes or voltage balancing capacitors is necessary.

III. SINGLE PHASE CASCADED MULTILEVEL INVERTERS

Four H-bridge modules are connected to the same dc input source in parallel, and each secondary of the four transformers is connected in series. In this configuration, the output voltage becomes the sum of the terminal voltages of each H-bridge module. The amplitude of the output voltage is determined by the input voltage and turn ratio of the transformer[2].

Usually, a traditional cascaded H-bridge converter employs a multipulse isolation transformer to obtain the input dc source. When the traditional cascaded H-bridge converter needs to isolate from the ac output, it requires a three-phase transformer between the inverter and the ac outputs. On the other hand, the proposed inverter has

an advantage of galvanic isolation between the source and the output voltages, which comes from being combined with transformers.[10][11]

IV. THREE PHASE CASCADED H-BRIDGE MULTILEVEL INVERTERS

Fig.2. shows a circuit configuration of the proposed multilevel inverter for three-phase applications. It consists of one single dc input source and several low-frequency three-phase transformers. By using the three-phase transformers, the number of transformers and the volume of system can be reduced. As a result, the price of the system is deservedly down.Each primary terminal of the transformer is connected to an H-bridge module so as to synthesize V_{dc} , zero, and $-V_{dc}$. Every secondary of the transformer is connected in series to pile the output level up. Moreover, each phase terminal is delta connected to restrain the third harmonic component[7].

In this configuration, each phase can be expressed independently, and we call each phase multilevel inverter as isolated H-bridge cascaded multilevel inverter. Therefore, the relationship between the input and the output voltages of the three-phase transformer is given as

$$\begin{bmatrix} V_{AK} \\ V_{BK} \\ V_{CK} \end{bmatrix} = \frac{T}{3} \cdot \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \cdot \begin{bmatrix} V_{ak} \\ V_{bk} \\ V_{ck} \end{bmatrix}$$
(1)

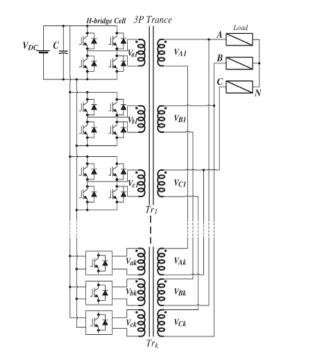


Fig.2. Circuit Configuration of Three Phase CMLI

where T is the transformation ratio (n2/n1) between the primary and the secondary of the transformer. If the input voltage is balanced in three phases, the sum of each phase voltage becomes zero

From (1) and (2), the output voltage is expressed as
$$\begin{bmatrix} V & AK \\ V & BK \\ V & CK \end{bmatrix} = T \cdot \begin{bmatrix} V & ak \\ V & bk \\ V & ck \end{bmatrix}$$
(2)

X7 X7 X7

From (3), we can notice that each phase output voltage of the transformer is given by the product of each phase input voltage and turn ratio of the transformer. However, in the proposed circuit configuration, it is often unbalanced in three phases because the primary of the transformer is connected to an H-bridge cell generating V_{dc} , zero, and $-V_{dc}$. It means that the output voltage is balanced at $V_{ak} = V_{DC}$, $V_{bk} = -V_{DC}$, and $V_{ck} = 0$; however, when V_{ak} , V_{bk} , and V_{ck} are all V_{DC} , the output voltage is unbalanced. Therefore, the proposed circuit relies on (1) instead of (3). Equation (1) has been expressed by the magnetic concept.

For example, a formed flux at the primary of phase "a" will be equally influenced on phases "b" and "c." Assuming that the quantity of the formed flux is two, the flux of both phases "b" and "c" becomes -1. By this concept, we can include the unbalanced relationship to (1). As shown in Fig.3., the output voltage of the proposed multilevel inverter is synthesized by the series-connected secondary of the transformer outputs. Hence, line voltages V_{AB} , V_{BC} , and V_{CA} can be given by

$$\begin{bmatrix} V_{AB} \\ V_{BC} \\ V_{CA} \end{bmatrix} = \begin{bmatrix} V_{AS} \\ V_{BS} \\ V_{CS} \end{bmatrix} = \begin{bmatrix} V_{A1+}V_{A2+\dots}V_{Ak} \\ V_{B1+}V_{B2+\dots}V_{Bk} \\ V_{C1+}V_{C2+\dots}V_{Ck} \end{bmatrix}$$
(4)

We can find that a diode-clamped multilevel inverter needs (M - 1).(M - 2).3 number of diodes to generate *M*-level outputs. In the case of a flying capacitor, it requires $[(M - 1)(M - 2) \times 3]/2 + (M - 1)$ number of capacitors for the generation of *M*-level outputs. A cascaded H-bridge inverter needs $[(M - 1)/2] \times 3 \times 4$ number of switches and $[(M - 1)/2] \times 3$ number of independent dc sources.

$$V_{AS} = \sum_{i=1}^{k} V_{Ai}$$

$$V_{BS} = \sum_{i=1}^{k} V_{Bi}$$

$$V_{CS} = \sum_{i=1}^{k} V_{Ci}$$
(5)

V. COMPARISON OF MULTILEVEL INVERTERS

Generally, the conventional multilevel inverters use a circulating switch pattern in order to maintain the same ratio in switch utilization. [10],[11].

Compo -nent	Diode clam ped	Flying capaci -tors	Conven -tional cascaded H-bridge	Proposed Cascaded H-bridge
Switch	36	36	72	36
Diode	396	0	0	0
Capacitor	4	210	18	1
Input DC source	1	1	18	1
Output transform er	1	1	1	4

Table: 1 Component Comparison of Nine Level Conventional Multilevel Inverters with the proposed ACMLI

Therefore, they employ switches which are equivalent in the voltage and current ratings. Assuming that the magnitude of the output voltages and output power are equivalent, the voltage ratings of each switch are determined by the number of series-connected switches. Consequently, we can say that the proposed method is

more advantageous in switch cost and system size compared with the conventional approaches because the proposed method can reduce the number of switches. In addition, usually, these traditional multilevel inverters employ a three-phase low-frequency transformer at the output terminal for a high-power grid connection. In this point, the proposed circuit topology has a valuable merit. Considering that the output voltage is synthesized by an accumulation of each transformer output, it does not require an additional transformer for galvanic isolation. Although the proposed scheme needs three three-phase transformers, the cost and size will be slightly increased because the capacity of the transformer is 1/3 of the transformer which is applied to the conventional method[1],[7].

VI. SIMULATION RESULTS

The conventional and the proposed multilevel inverter are designed and simulated using MATLAB/Simulink tool. The PWM scheme employed to control the inverter is the single phase cascaded multilevel inverter is analyzed based on different loading conditions. Fig 4 represents the output voltage of the single phase cascaded multilevel inverter when running a pure resistive load and RL load of about 1kW. This can be eliminated by using proper harmonic filter circuit. Fig.4 and 5 represents the output voltage with R and RL load without any filter circuit. Also Fig.6. and 7 holds the harmonic spectra of the output voltage with R and RL load of about 1 kW respectively.

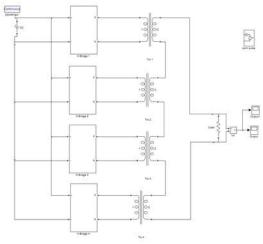


Fig .3. Simulation Model for single phase ACMLI

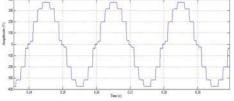
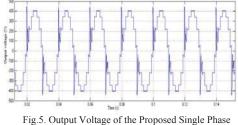


Fig.4. Output Voltage of the Proposed Single Phase ACMLI With pure R Load



5. Output Voltage of the Proposed Single Phase CMLI with RL load- 1kW

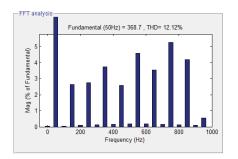


Fig.6. Harmonic Spectrum of the Single Phase ACMLI Output Voltage with Pure R load

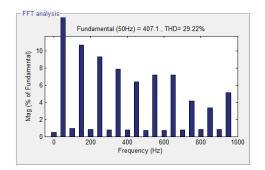
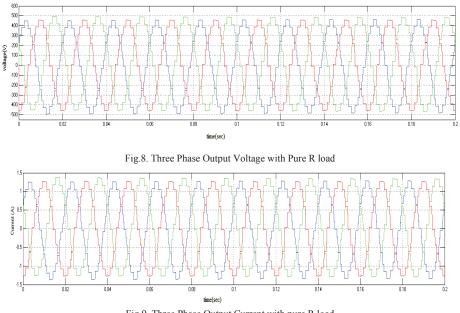


Fig.7. Harmonic Spectrum of the Single Phase ACMLI output voltage with RL Load

The performance of the three phase cascaded multilevel inverter with single dc input is analyzed under different loading conditions. The output voltage and current obtained when driving a pure resistive load is given in Fig.8 and 9.





The corresponding harmonic spectrum of the three phase cascaded multilevel inverter at R load with respect to voltage and current is given in Fig.10 and 11.

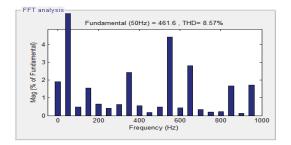


Fig.10. Harmonic Spectrum of Three Phase ACMLI Output Voltage with pure R load

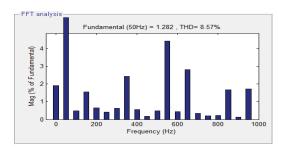


Fig.11. Harmonic Spectrum of Three PhaseACMLI output current with RL load

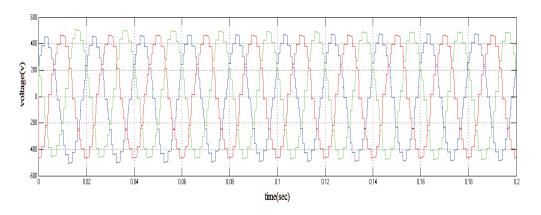


Fig.12. Three phase Output Voltage with RL Load of 1kW

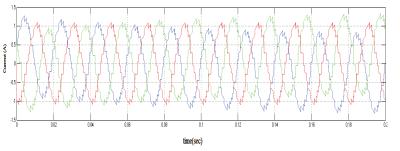
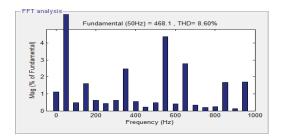


Fig.13. Three phase Output Current with RL Load of 1kW

The corresponding harmonic spectrum and % of THD in the output voltage and current when driving an r and RL load of 1kW is depicted in 14 and 15.



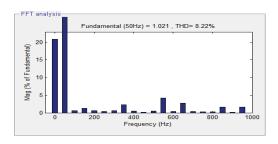


Fig.14. Output voltage THD when Driving RL Load of 1kW 1kW

Fig.15. Output Current THD when Driving RL Load of

It is seen that the single phase CMLI and three phase CMLI with pure R load and RL load of about 1kW has been simulated using MATLAB under various loading conditions. The inverter output is a nine level output voltage with having 4 legs. In the proposed ACMLI, the number of switches used to get the nine level output voltage is comparatively less than that of the other conventional types of multilevel inverters. Hence the switching loss and stress is also reduced to about 50% in comparison with the normal CMLI, which in turn reduces the cost, circuit simplexity,THD, reliability, etc.

VII. HARDWARE RESULTS

Fig.16. shows the hardware implementation of the proposed ACMLI under different loading conditions. Initially, a single DC source is gaiven as the input to the 4 legs of H bridge Inverters which in turn consists of switches. A suitable isolation transformers will be used to provide the isolation purpose.

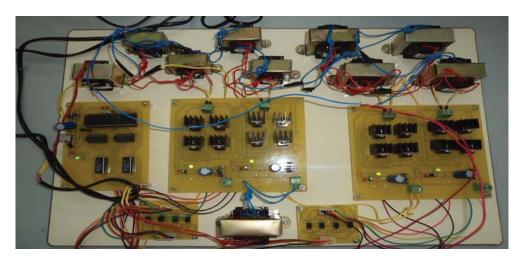


Fig.16. Hardware Implementation of ACMLI - top view

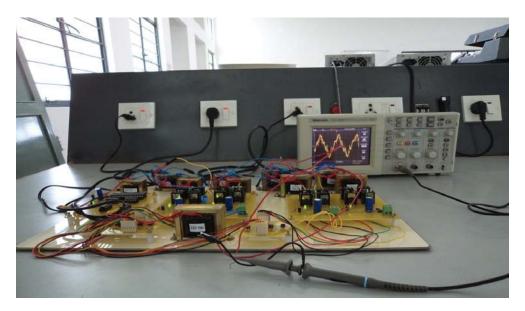


Fig.17. Experimental setup of ACMLI with simple R load

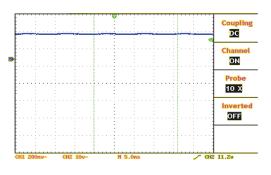


Fig.18. DC input voltage



Fig.19. Output Voltage with 1kW R load

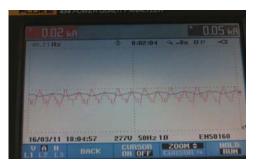


Fig.20. Output Current with 1kW R load

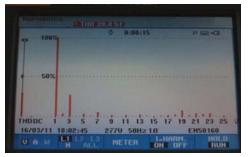


Fig.21. Output Voltage THD with R load



Fig.22. Output Current THD with R load

VIII. CONCLUSION

In this work, a nine level ACMLI for renewable energy applications has been proposed. Simulation were done using MATLAB R2010/Simulink toolbox and hardware results were also presented. The proposed nine level cascaded multilevel inverter is simulated using single dc source. The THD values of both current and voltage parameters has been reduced comparatively with the conventional multi level inverter topology. Also the reduction in number of dc source also adds advantage to the system. Consequently, the efficiency of the system improves relatively with the conventional multilevel inverter configuration.

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