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Experimentation of Boost Chopper Interfaced Cascaded Multilevel Inverter Topology for Photovoltaic Applications

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Abstract – *This paper presents the experimentation of Cascaded Multilevel Inverter (CMLI) for Photo Voltaic (PV) generator feeding an isolated load. For the improvement of PV system utilization, boost chopper interfaced CMLI configuration is developed under Multicarrier Sinusoidal Pulse Width Modulation (MCSPWM) control schemes. Boost chopper interfaced CMLI configuration boost up the PV panel voltage and generates high quality of AC power for domestic and drive load applications. The entire systems of PV, boost chopper and CMLI are simulated using SIMULINK and the results are validated. Prototype hardware model of single phase boost chopper interfaced 7-Level CMLI configuration is developed and its output illustrations are validated.*

Keywords: *Boost Chopper, Cascaded Multilevel Inverter, Photo Voltaic, Pulse Width Modulation*

Nomenclature

AC	Alternating Current
DC	Direct Current
PV	Photo Voltaic
D	Duty cycle
CMLI	Cascaded Multilevel Inverter
MCSPWM	Multicarrier Sinusoidal Pulse Width Modulation
N	Number of levels
V_{DC}	Boost chopper input DC voltage
V_O	Boost chopper output DC voltage
V_{AC}	Inverter output AC voltage
I_{dc}	Boost chopper input current
I_s	Inverter Input current
I_o	Inverter output current
T_{ON}	Chopper switch ON time
T_{OFF}	Chopper switch OFF time

I. Introduction

Solid state power semi converter devices have the responsibility to interface the renewable resources with the utility. Different families of power converters have been designed to utilize the renewable resources for various applications. Nowadays solar PV system installation involves the use of multiple series and parallel connected solar panels with CMLI topology [1]-[5]. In this paper, PV panels are integrated with boost chopper and CMLI topology and its performance is investigated with respect to output voltage, load current and Total Harmonic Distortion (THD) [6]-[8]. This paper is organized as follows; Section I shows the introduction of CMLI configurations. Analysis of boost chopper interfaced CMLI configuration is reviewed in Section II.

Simulation of boost chopper interfaced CMLI configuration is evaluated in Section III. Simulation results are discussed in Section IV. An experimental analysis of boost chopper interfaced CMLI configuration is addressed in Section V.

Finally, Section VI concludes the paper. The general block diagram of CMLI fed solar powered AC load system is shown in Fig. 1. Generally, CMLI system required more number of battery count and series-parallel connected DC sources.

Fig. 2 shows the block diagram of boost chopper interfaced CMLI system configuration. Generally, boost operation can be carried out by linear transformer. In this work, linear transformer is replaced by boost chopper circuit.

Boost chopper circuit boosts up the PV system voltage via battery banks. Through boost chopper interfaced CMLI configuration, battery count and DC source count can be reduced with desired battery backup period.

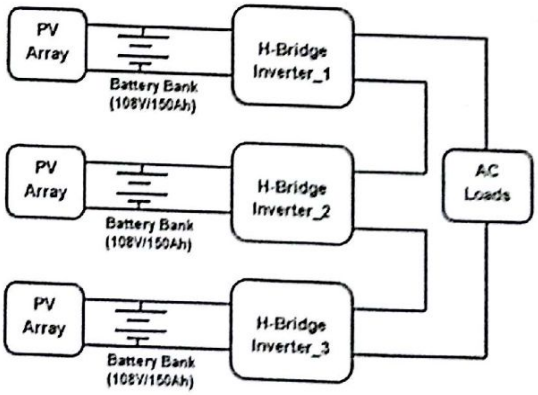

Fig. 1. Block diagram of CMLI

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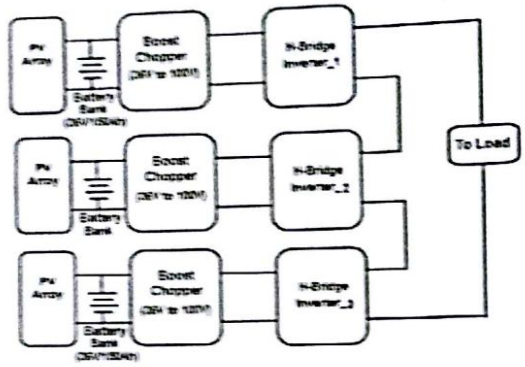


Fig. 2. Block diagram of boost chopper interfaced CMLI

II. Analysis of Boost Chopper Interfaced CMLI Configuration

CMLI system composed of series of H-Bridge power cells, which are well suited for reactive power compensation.

To reduce series connected source count, boost chopper is interfaced between DC source and inverter unit as shown in Fig. 3(a).

The handling of boost chopper circuit is better than battery banks and linear transformer. Each H-Bridge of CMLI has separate equivalent PV systems, which is interconnected with each other in series manner through proper switching of CMLI [9]-[13].

II.1. Modes of Operation

Mode 1 and Mode 3

In this mode, boost chopper switches SB1, SB2 and SB3 are in ON state. When the boost chopper switches are in ON state, corresponding inductors L_1, L_2 and L_3 get energized and the diodes D_1, D_2 and D_3 are in OFF state. In this mode all the H-Bridge switches are in OFF state. The equivalent circuit for these modes of operation is shown in Fig. 3(b).

Mode 2

In this mode, boost chopper switches SB1, SB2 and SB3 are in OFF state. Energy stored in the inductors L_1, L_2 and L_3 at mode 1 are now get de-energized through the diodes D_1, D_2 and D_3 and H-Bridge switches.

To obtain positive cycle of AC voltage across the load, H-Bridge switches S_1, S_2, S_5, S_8, S_9 and S_{11} are get activated and other H-Bridge switches S_3, S_4, S_7, S_8, S_{11} and S_{12} switches are get deactivated. In this mode, load get utilize the source power (solar power) and inductor power.

The equivalent circuit and load current direction Io of mode 2 operation is shown in Fig. 3(c).

Mode 3

Operation of mode 3 is similar to that of mode 1 operation.

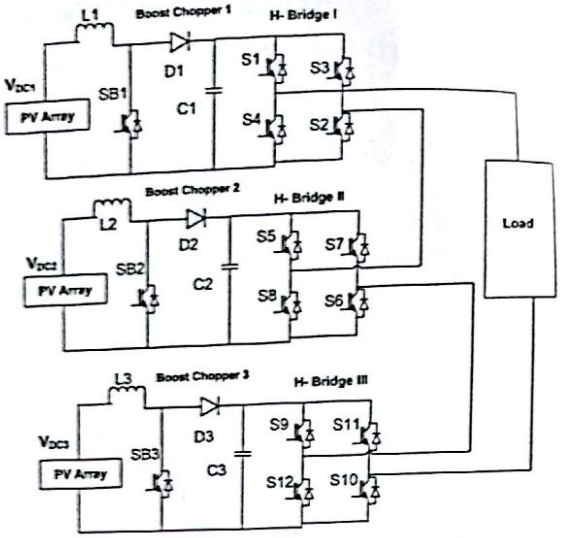


Fig. 3(a). Structure of boost chopper interfaced CMLI

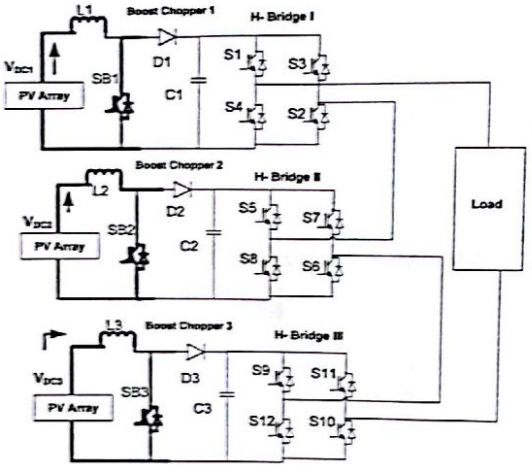


Fig. 3(b). Equivalent structure of mode 1 and mode 3 operation

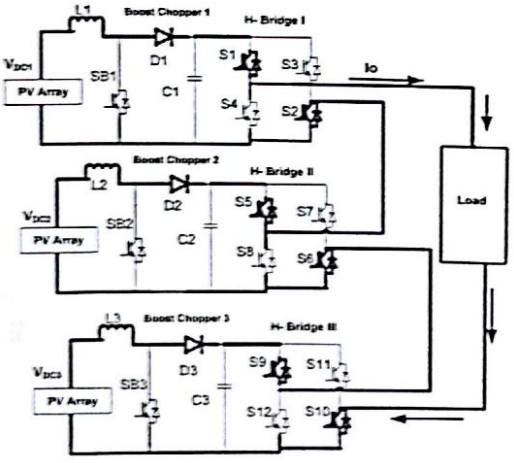


Fig. 3(c). Equivalent structure of mode 2 operation

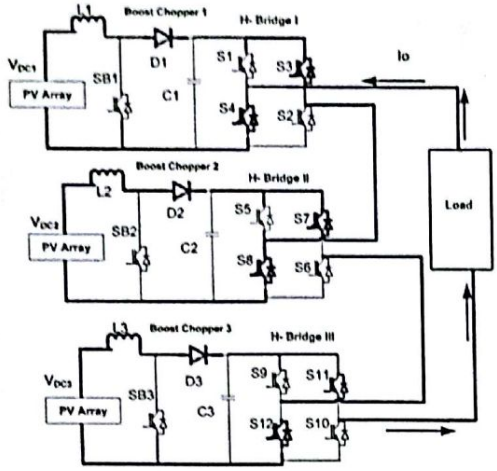


Fig. 3(d). Equivalent structure of mode 4 operation

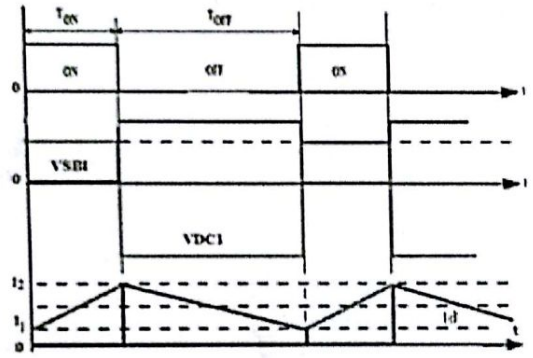


Fig. 3(e). Switching states and change in inductor current waveform of boost chopper circuit 1

Mode 4

In this mode, boost chopper switches SB1, SB2 and SB3 are in OFF state. Energy stored in the inductors L_1, L_2 and L_3 at mode 3 are now get de-energized through the diodes D_1, D_2 and D_3 and H-Bridge switches To obtain negative cycle of AC voltage across the load, H-Bridge switches S_3, S_4, S_7, S_8, S_{11} and S_{12} are get activated and other H-Bridge switches S_1, S_2, S_5, S_6, S_9 and S_{10} are get deactivated.

In this mode also, load get utilize the source power (solar power) and inductor power. The equivalent circuit and load current direction Io of mode 4 operation is shown in Fig. 3(d).

II.2. Analysis

During T_{ON1}, the inductor (L_1) current rises linearly from I_1 to I_2 can be expressed in equation (1) and shown in Fig. 3(e). The ON time of SB1 is written as equation (2):

$$V_{DC1} = L_1 \frac{I_2 - I_1}{T_{ON}} \tag{1}$$

$$T_{ON1} = L_1 \frac{I_2 - I_1}{V_{DC1}} \tag{2}$$

During T_{ON2}, the inductor (L_2) current rises linearly from I_3 to I_4 can be expressed in equation (3) and shown in Fig. 3(f) The ON time of SB2 is written as equation (4):

$$V_{DC2} = L_2 \frac{I_4 - I_3}{T_{ON}} \tag{3}$$

$$T_{ON2} = L_2 \frac{I_4 - I_3}{V_{DC2}} \tag{4}$$

During T_{ON3}, the inductor (L_3) current rises linearly from I_5 to I_6 can be expressed as equation (5) and shown in Fig. 3(g). The ON time of SB3 is written as equation (6):

$$V_{DC3} = L_3 \frac{I_6 - I_5}{T_{ON}} \tag{5}$$

$$T_{ON3} = L_3 \frac{I_6 - I_5}{V_{Dc3}} \tag{6}$$

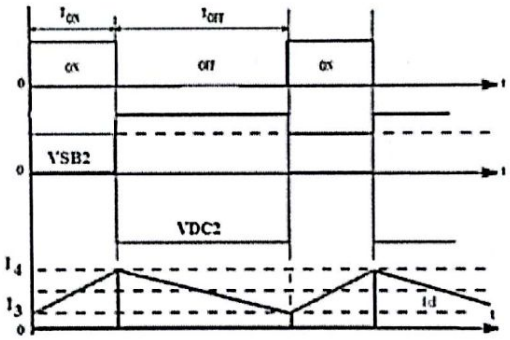


Fig. 3(f). Switching states and change in inductor current waveform of boost chopper circuit 2

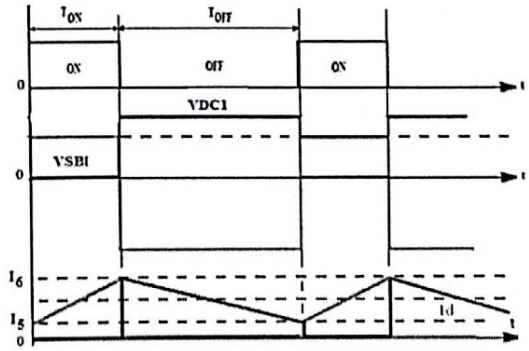


Fig. 3 (g). Switching states and change in inductor current waveform of boost chopper circuit 3

The output voltage of boost chopper circuits can be expressed as equations (7), (8) and (9):

$$V_{out1} = \frac{V_{DC1}}{1-D} \quad (7)$$

$$V_{out2} = \frac{V_{DC2}}{1-D} \quad (8)$$

$$V_{ou3} = \frac{V_{DC3}}{1-D} \quad (9)$$

The duty cycle of boost chopper circuit can be expressed in equation (10):

$$D = \frac{T_{ON}}{T} \quad (10)$$

The AC output voltage of CMLI can be expressed in equation (11):

$$V_{AC} = \frac{N-1}{2} \cdot V_{out} \quad (11)$$

where:

$$V_{out} = V_{out1} = V_{out2} = V_{out3}$$

The output current of chopper circuits can be expressed as equations (12), (13) and (14):

$$I_{dc1} = (1-D) \cdot I_{S1} \quad (12)$$

$$I_{dc2} = (1-D) \cdot I_{S2} \quad (13)$$

$$I_{dc3} = (1-D) \cdot I_{S3} \quad (14)$$

where:
V_{DC} is the input voltage to the boost chopper circuit;
V_{out} is the boost chopper output voltage;
I_{dc} is the input current of boost chopper circuit;
D is the boost chopper duty cycle;
N is the number of levels of the multilevel inverter;
V_{AC} is output voltage of CMLI;
I_S is the input current of inverter circuit;
I_O is the output current of inverter circuit.

TABLE I
COMPARATIVE ANALYSIS BETWEEN CONVENTIONAL CMLI AND BOOST CHOPPER INTERFACED CMLI

Parameters	Conventional solar powered CMLI	Boost Chopper Interfaced solar powered CMLI
Source Count (Solar Panel 12 V, 16 A)	18	9
Battery Count	18	9
Battery Backup Period (For 500 W restive Load)	3 Days	32 Hrs
Battery Back Up Period (For 2.5 kW drive Load)	15Hrs	7 Hrs

Parameter Analysis:

Comparative analysis of source count, battery count and back up period between conventional CMLI and boost chopper interfaced CMLI are arrayed in Table I. From the analysis it is inferred that the number of source count and battery count in the boost chopper interfaced CMLI system is 50% as compared to that of conventional CMLI topology.

Conventional 7-Level CMLI system required 100 V input for each H-Bridge of CMLI. So, the number of battery count in the conventional CMLI is eighteen irrespective of the load rating and backup periods. But, in boost chopper interfaced 7-Level CMLI boost chopper circuit decides the battery count and backup period for desired applications.

Better quality of power is obtained through proper switching of inverter switches [14]-[21].

III. Simulation of CMLI Configuration

III.1. Modeling of PV Panels

Fig. 4 shows the modeling of PV panels. Solar cells are integrated and simulated using SIMULINK.

Each module is modeled for 12 V, 16 A at the solar irradiation of 1000W/m^2 and at the panel temperature of 25°C. Three PV modules are connected in series to obtain the output voltage of 36 V.

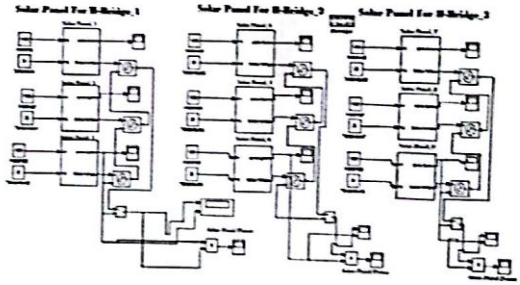


Fig. 4. Modeling of PV panels

III.2. Simulation of PV Integrated Boost Chopper Interfaced Single Phase CMLI Systems

Fig. 5 shows the simulation model of PV panel integrated boost chopper interfaced upper H-Bridge CMLI configuration. The output voltage of PV panel (36 V) is used to charge 12 V/150 Ah battery bank. The battery output is boosted to 100 V using boost chopper unit with the duty cycle of D.

The obtained output voltage is fed to CMLI unit. To obtain desired 7-level AC output voltage, all the three H-Bridges of CMLI are designed in similar manner.

Fig. 6 shows the overall simulation model of MCSPWM switching based boost chopper interfaced CMLI configuration for drive load applications. Input and output parameters of the entire system are analyzed and the results are discussed in further sections.

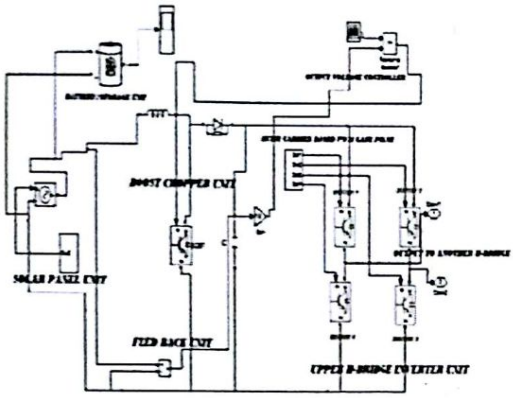


Fig. 5. Simulation of boost chopper interfaced CMLI (upper H-bridge)

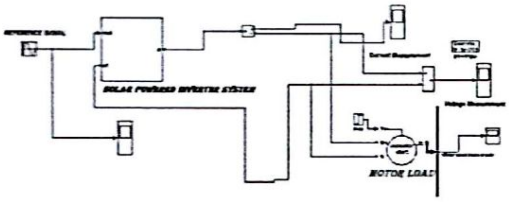


Fig. 6. Over all simulation of boost chopper interfaced single phase CMLI fed induction motor drive

III.3. Simulation of PV Integrated Boost Chopper Interfaced Three Phase CMLI Systems

Fig. 7 shows the overall simulation model of MCSPWM switching based CMLI configuration fed three phase induction motor drive. In this simulation model, nine H-Bridges are integrated to obtain 7- level, 415 V, 3ϕ, 50Hz, AC output voltage of induction motor drive applications. Electrical and mechanical parameters of induction motor drive are analyzed in section IV.

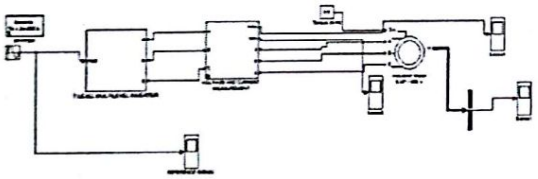


Fig. 7. Over all simulation of boost chopper interfaced three phase CMLI configuration fed induction motor drive

IV. Simulation Results and Discussion of CMLI Configuration

IV.1. Evaluation of Solar PV Panel Results and Boost Chopper Unit Results

Fig. 8 shows the output voltage (36 V) and output current (16 A) of PV system at the surface temperature of 25 °C and solar irradiance of 1000 W/m^2. The obtained output voltage of 36 V is boosted to 108 V using boost chopper.

Fig. 9 shows the firing pulse pattern to boost chopper circuit. The switching frequency of the chopper is 1 kHz with the duty cycle (D) of 0.65.

Fig. 10 shows the input and output voltage of boost chopper circuit. Solar PV voltage of 36 V is fed to boost chopper via battery bank, and it is boosted to 100 V.

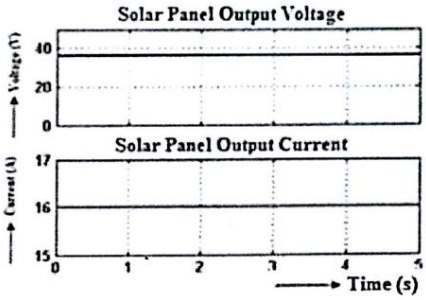


Fig. 8. Solar PV output voltage and current

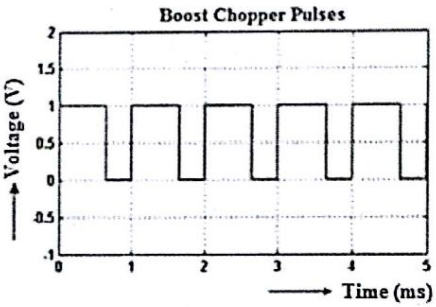


Fig. 9. Firing pulses to boost chopper switch

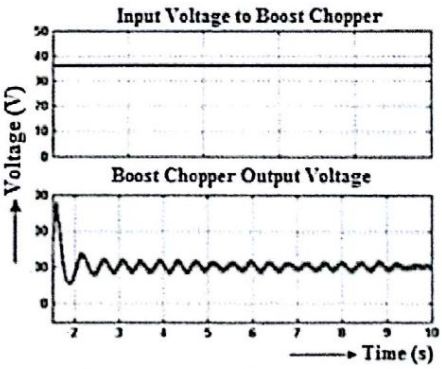
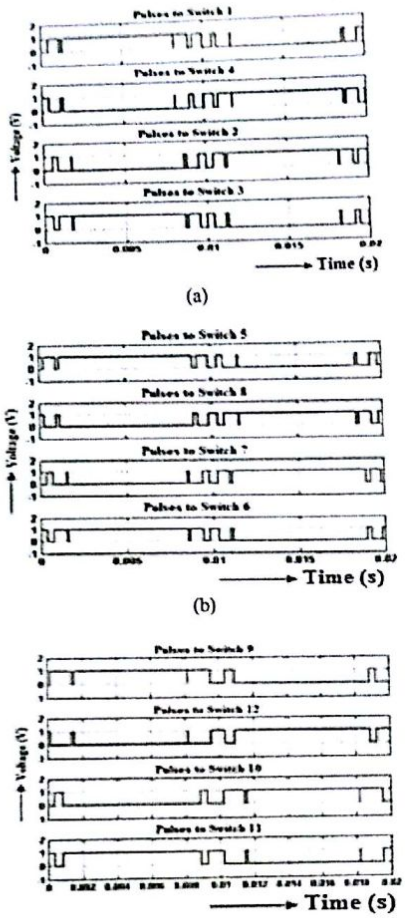


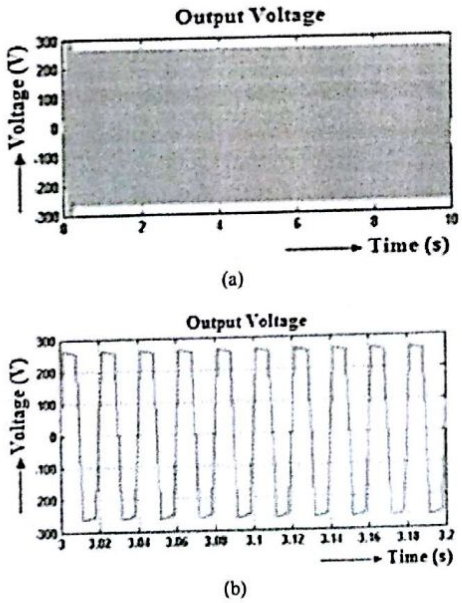
Fig. 10. Input and output voltage waveforms of chopper unit

IV.2. Evaluation of CMLI Unit Results

MCSPWM based firing pulses patterns are shown in Figs. 11(a), (b) and (c). MCSPWM pulses provide good power quality output of voltage and current. Figs. 12(a) and (b) show the output voltage waveform (Vmax=280 V) of boost chopper interfaced CMLI fed single phase resistive load with the output frequency of 50 Hz.



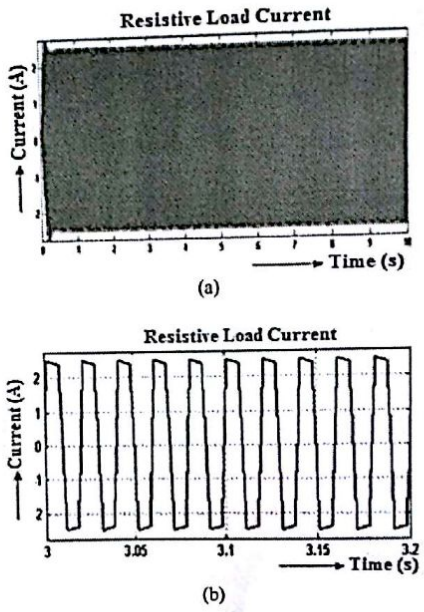
Figs. 11. Switching pulses to CMLI switches: (a) To switches 1 to 4 (b) To switches 5 to 8 (c) To switches 9 to 12



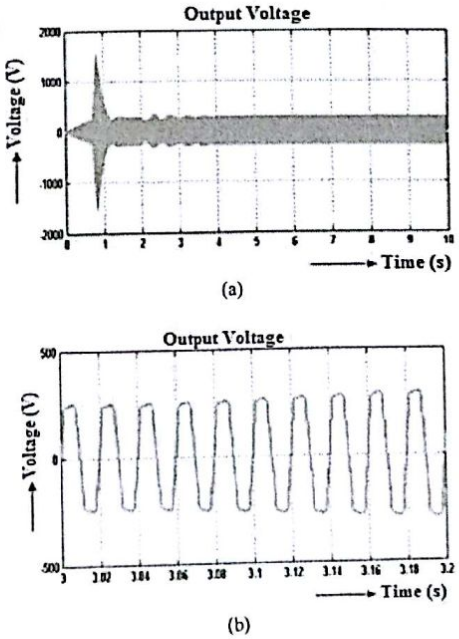
Figs. 12. (a) Output voltage waveform of CMLI fed resistive load, (b) Magnified portion (3 to 3.2 seconds) of output voltage

Figs. 13(a) and (b) show the load current waveform (I_L=2.5 A) of boost chopper interfaced CMLI fed single phase resistive load with the output frequency of 50 Hz.

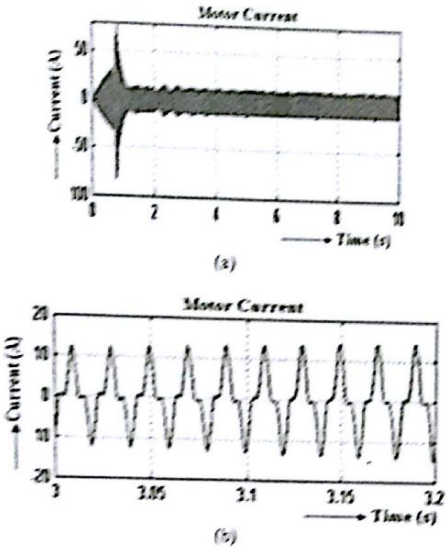
Figs. 14 (a) and (b) show the output voltage waveform (V_{max}=337 V) of boost chopper interfaced CMLI fed single phase induction motor drive with the output frequency of 50 Hz. Figs. 15(a) and (b) show the current waveform (I_L=12 A) of boost chopper interfaced CMLI fed single phase induction motor drive with the output frequency of 50 Hz.



Figs. 13. (a) Output load current waveform of CMLI fed resistive load system, (b) Magnified portion (3 to 3.2 seconds) of output current



Figs. 14. (a) Output voltage waveform of CMLI fed induction motor drive, (b) Magnified portion (3 to 3.2 seconds) of output voltage



Figs. 15. (a) Output load current waveform of CMLI fed induction motor drive, (b) Magnified portion (3 to 3.2 seconds) of output current

Fig. 16 shows the rotor speed of (1480 RPM) single phase induction motor drive, which is driven by solar powered 7-Level boost chopper interfaced CMLI system.

Figs. 17(a) and (b) show the THD spectrum of 7-Level CMLI fed single phase induction motor drive.

From the spectrum, it is viewed that the fundamental harmonics is 100%, 3rd order harmonics is 17.6%, 5th order harmonics is 0.83%, 7th order harmonics is 3.03%, 9th order harmonics is 1.82%, 11th order harmonics is 0.15%, 13th order harmonics is 0.09% and over all distortion is 18.27%. From the analysis, it is observed that in single phase system only third order harmonics is more dominant than other harmonics. As per IEEE standard 519:1992, the value of individual harmonics should be less than 3%. So, LC filter is recommended to eliminate the third order harmonics. The L and C value of filter circuit is 11.2 mH and 900 μF respectively.

Figs. 18(a) and (b) show the THD spectrum of 7-level CMLI fed single phase induction motor drive with LC filter. From the spectrum, it is viewed that the fundamental harmonics is 100%, 3rd order harmonics is 3.09%, 5th order harmonics is 0.16%, 7th order harmonics is 0.08%, 9th order harmonics is 0.03%, 11th order harmonics is 0.02%, 13th order harmonics is 0.01% and over all distortion is 3.15%.

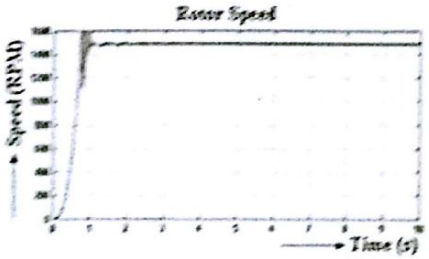
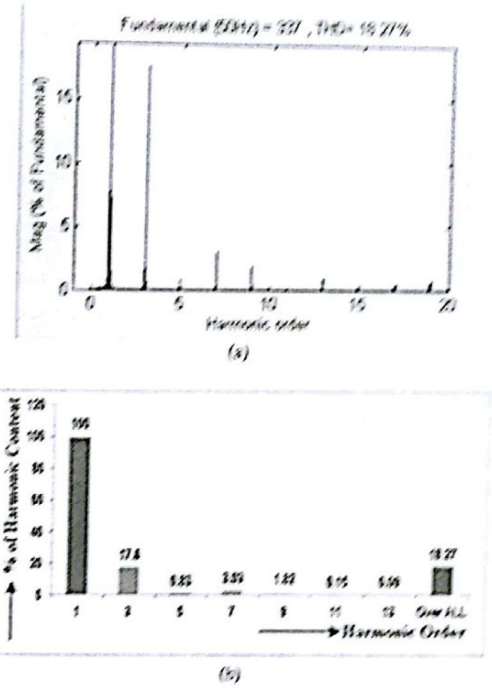
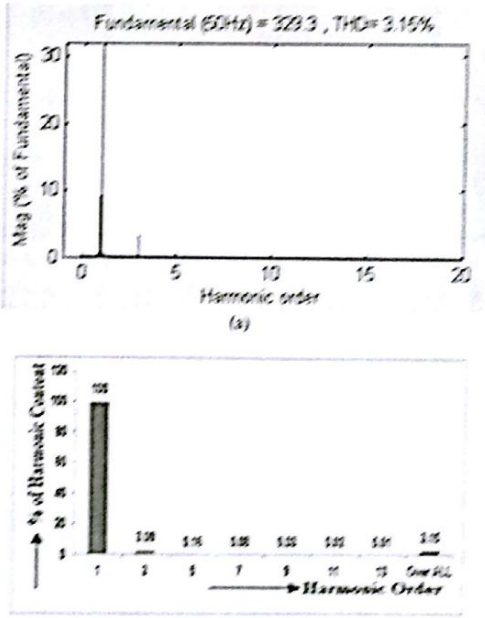


Fig. 14. Single phase induction motor drive speed in RPM



Figs. 17. THD analysis (a) Spectrum analysis (18.27%) (b) Individual harmonic analysis



Figs. 18. THD analysis with LC filter (a) Spectrum analysis (3.15%), (b) Individual harmonic analysis

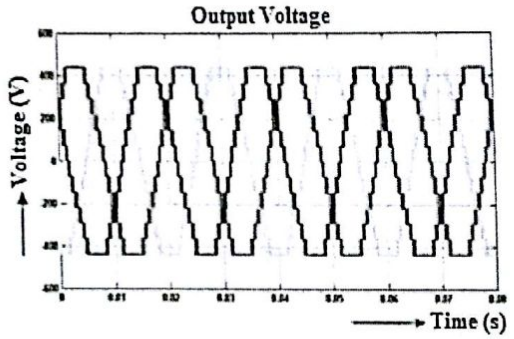
From the analysis, it is understood that third order harmonics is reduced to 3.15%. As per IEEE standard 519:1992, the overall THD value should be less than5%. The obtained results satisfy the IEEE standard.

The output line voltage (440 V) and 50 Hz frequency of MCSPWM switching based 7-level boost chopper interfaced CMLI fed three phase induction motor drive is shown in Fig. 19(a).

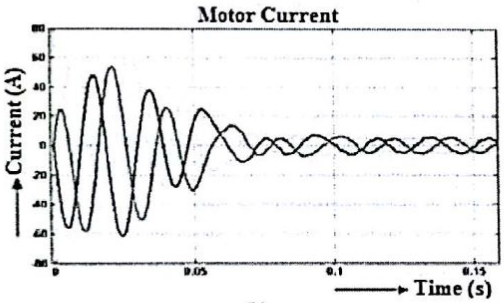
Fig. 19(b) shows the output drive current (6 A) of 7-level CMLI fed three phase induction motor drive at the load condition of 5 N-M.

Fig. 20 shows the rotor speed of (1390 rpm) three phase induction motor drive, which is driven by solar powered 7-level boost chopper interfaced CMLI system.

Fig. 21 shows the THD spectrum of 7-level CMLI fed three phase induction motor drive. From the spectrum, it is viewed that the fundamental harmonics is 100%, 3rd order harmonics is completely eliminated, 5th order harmonics is 2%, 7th order harmonics is 2.5% and over all distortion is 8.43%. Individual harmonics satisfy.



(a)



(b)

Figs. 19. (a) Voltage waveform of three phase CMLI fed induction motor drive (b) Drive current waveform for (mechanical load of 5N-M)

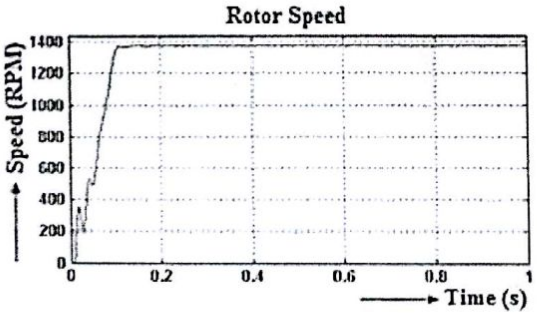


Fig. 20. Three phase induction motor drive speed in RPM

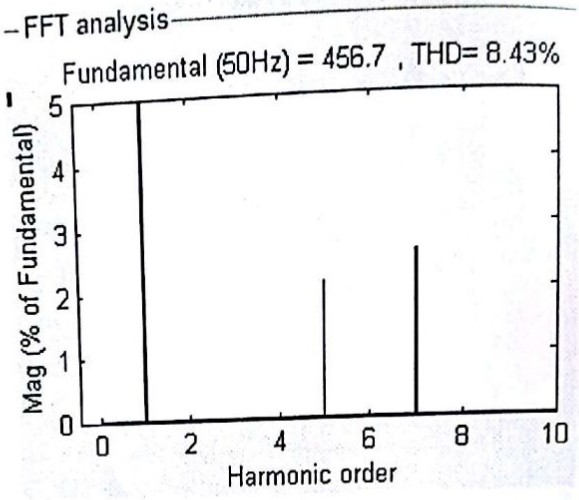


Fig. 21. THD spectrum analysis (8.43%)

V. Experimental Analysis of Boost Chopper Interfaced CMLI Configuration

V.1. Schematic Circuit of Boost Chopper Interfaced CMLI Fed Single Phase R-Load System

Fig. 22 shows the hardware circuit of 7-level boost chopper interfaced CMLI fed single phase resistive load system.

The equivalent circuit consists of power supply unit, micro controller unit (PIC16F877), opto coupler uint, driver uint (IR2110), boost converter unit and H-bridge inverter uint.

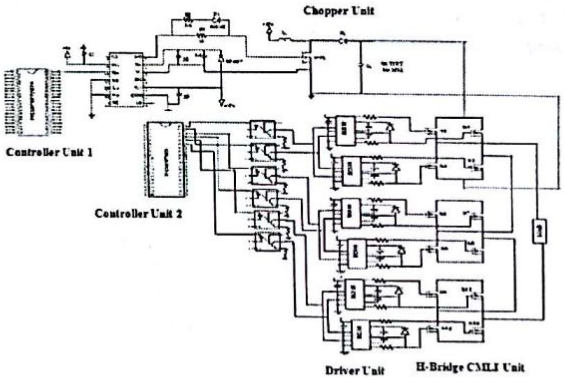


Fig. 22. Overall hardware circuit of MCSPWM switching based 7-level CMLI fed R-load

V.2. Results and Discussion

Boost chopper boost up the battery output voltage of 36 V to 85 V shown in the Fig. 23.

The obtained output is fed to one of the H-bridge of CMLI unit to synthesize an AC output voltage. Similarly other two H-bridges of CMLI unit gets the input supply from boost chopper unit and synthesize AC output voltage.

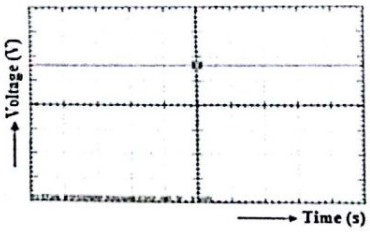
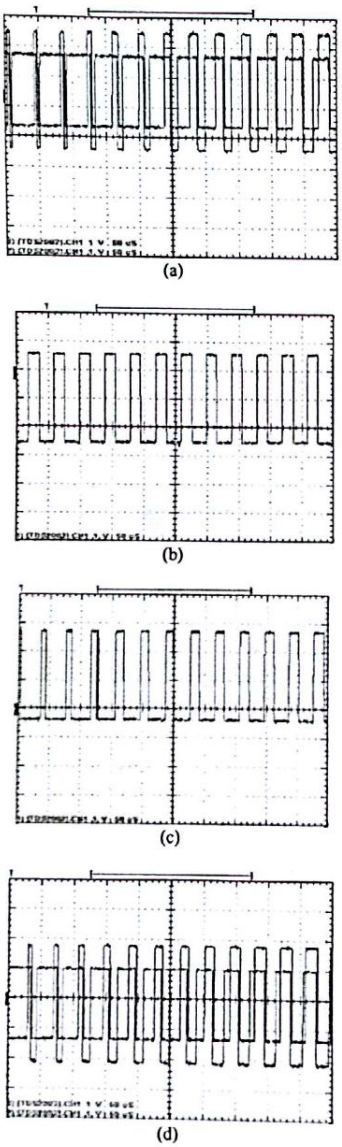


Fig. 23. Boost chopper output voltage (85V)



Scale: X axis 1 unit = 50μS, Y axis 1 unit = 1 V

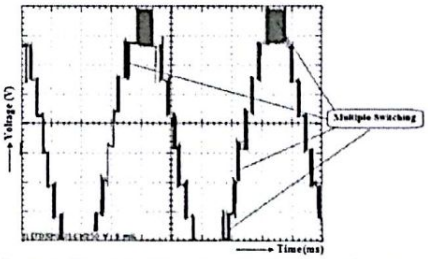
Figs. 24. MCSPWM pattern to H-bridge switches: (a) Pulse pattern to switches 1,2, 5and 6 (b) Pulse pattern to switches 9and 10 (c) Pulse pattern to switches 3 and 4 (d) Pulse pattern to switches 7, 8, 11and 12

MCSPWM based switching pattern of inverter switches are shown in Figs. 24(a), (b), (c) and (d).

This switching pattern provides quality output voltage.

The output voltage of (200 V, 50 Hz) single phase seven level boost chopper interfaced CMLI fed resistive load system is shown in Fig. 25. It is clearly viewed that the stair case output voltage is structured by several multiple switching of inverter switches.

Figs. 26(a) and (b) show the prototype mode of proposed system. The entire system is assembled in a single board and input voltage is obtained from DC power supply unit. The entire unit is tested for various light loads.



Scale: In X- axis 1 unit = 50 ms, In Y-axis 1 unit =50 V

Fig. 25. Output voltage (200V) of boost chopper interfaced CMLI fed resistive load

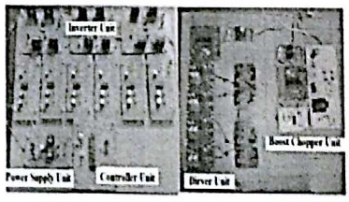


Fig. 26(a). Experimental setup of single phase seven level boost chopper interfaced CMLI

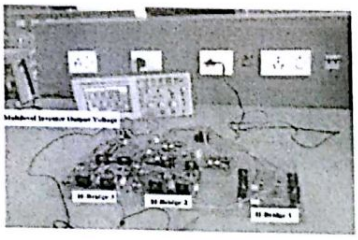


Fig. 26(b). Prototype model of seven-level boost interfaced CMLI with measuring DSO

VI. Conclusion

Through this work, boost chopper interfaced single phase seven- level CMLI configuration is designed, fabricated and tested. Compared to conventional CMLI, series connected source count and battery count is reduced in boost chopper interfaced CMLI.

Better quality of AC output voltage of CMLI system is achieved through MCSPWM switching strategy. This

CMLI configuration can be adopted for domestic UPS systems and industrial drives with desired backup periods. Simulated results and hard results are compared and validated. The obtained THD value of output voltage of single phase boost cascaded CMLI is 3.15 % and the individual harmonic content of output voltage of three phase boost cascaded CMLI is less than 3%, which both satisfy the IEEE 519:1992 standard.

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