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Question Paper Code : 73374

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2017.

Third Semester

Computer Science and Engineering

CS 2202/CS 34/EC 1206 A/10144 CS 303/080230012 — DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Information Technology)

(Regulations 2008/2010)

(Also common to PTCS 2202 – Digital Principles and System Design for B.E. (Part-Time) Second Semester – CSE – Regulations 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Convert $(1001010.1101001)_2$ to base 16 and $(231.07)_8$ to base 10.

2. Realize XOR gate using only 4 NAND gates.

3. Give the truth table for half adder and write the expression for sum and carry.

4. Write any two advantages of HDL.

5. Distinguish between a decoder and a demultiplexer.

6. Compare SRAM and DRAM.

7. Distinguish between synchronous sequential circuits and asynchronous sequential circuits.

8. How many logic devices are required for a MOD-64 parallel counter?

9. Distinguish between a conventional flow chart and an ASM chart.

10. Draw the block diagram of an asynchronous sequential circuit.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Simplify F(A, B, C, D) = Σ (0, 1, 2, 5, 8, 9, 10) in sum of products and product of sums using K-map. (12)

(ii) Write notes on negative and positive logic. (4)

Or

(b) (i) Simplify the expression F(A, B, C, D) = Σ(1, 4, 6, 7, 8, 9, 10, 11, 15) using Quine-McClusky method. (12)

(ii) Check if NOR operator is associative. (4)

12. (a) (i) With the neat diagram, discuss the working principle of carry look-ahead adder. (11)

(ii) Design a 4-bit adder using three full adders and one half adder. (5)

Or

(b) (i) Write the VHDL code for BCD-to-7 segment code convertors, using a selected signal assignment. (12)

(ii) Write test bench for half adder circuit. (4)

13. (a) Implement the following Boolean function using 8:1 multiplexer. (16)

F (A, B, C, D) = A'BD' + ACD + B'CD+A'C'D

Or

(b) Implement the following Boolean functions using PAL. (16)

w (A, B, C, D) = Σm (0, 2, 6, 7, 8, 9, 12, 13)

x (A, B, C, D) = Σm (0, 2, 6, 7, 8, 9, 12, 13, 14)

y (A, B, C, D) = Σm (2, 3, 8, 9, 10, 12, 13)

z (A, B, C, D) = Σm (1, 3, 4, 6, 9, 12, 14).

14. (a) Using D flip-flops, design a synchronous counter which counts in the sequence, 000, 001, 010, 011, 100, 101, 110,111, 000.

Or

(b) Design a shift register using JK flipflops.

15. (a) (i) What is the objective of state assignment in asynchronous circuit? Explain race-free state assignment with an example (8)

(ii) Discuss about static, dynamic and essential hazards in asynchronous sequential circuits. (8)

Or

(b) Design an asynchronous sequential circuit with inputs x1 and x2 and one output z. Initially, and at any time if both the inputs are 0, output is equal to 0. When x1 or x2 becomes 1, z becomes 1. When second input also becomes 1, z = 0; The output stays at 0 until circuit goes back to initial state. (16)

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