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**Question Paper Code : 50380**

**B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2017**

**Second Semester**

**Computer Science and Engineering**

**CS6201 – DIGITAL PRINCIPLES AND SYSTEM DESIGN**

**(Common to Information Technology)**

**(Regulations 2013)**

**Time : Three Hours**

**Maximum : 100 Marks**

**Answer ALL questions.**

**PART – A**

**(10×2=20 Marks)**

1. What is meant by self-complementing code ?
2. What are the limitations of K-Map ?
3. What are binary decoders ?
4. Write the truth table of full subtractor.
5. How synchronous counters differ from asynchronous counters ?
6. What is edge-triggered flip-flop ?
7. Define Merger graph.
8. What is critical and non-critical race ?
9. What is memory decoding ?
10. What is programmable logic array ? How it differs from ROM ?

**PART – B**

**(5×16=80 Marks)**

11. a) Simplify the following expressions and implement them with two-level NAND gate circuits :

i)  $AB' + ABD + ABD' + A'C'D' + A'BC'$

ii)  $BD + BCD' + AB'C'D'$

**(OR)**



b) Simplify the following expressions in (1) sum of the products and (2) products of sums :

i)  $x'z' + y'z' + yz' + xy$

ii)  $AC' + B'D + A'CD + ABCD$

iii)  $(A' + B' + D')(A + B' + C')(A' + B + D')(B + C' + D')$

12. a) Design and implement binary to gray code convertor.

(OR)

b) Implement the switching function  $F(A, B, C, D) = \Sigma (0, 1, 3, 4, 12, 14, 15)$  using 8:1 multiplexer.

13. a) Explain the operation of JK FF, SR-FF, T-FF and D-FF with a neat diagram. Also discuss their characteristic equation and excitation table.

(OR)

b) Design Mod-7 counter using JK flip-flop.

14. a) Explain about the designing of Asynchronous sequential circuits with example.

(OR)

b) What are Hazards and its types ? How can you design a hazard free circuit, explain with example ?

15. a) Explain about error detection and correction using hamming codes.

(OR)

b) Explain in detail about the Programmable Logic Array, Programmable Array Logic.