Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 52855

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2019.

Second Semester

Computer Science and Engineering

CS 6201 – DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Information Technology)

(Regulation 2013)

(Also Common to PTCS 6201 – Digital Principles and System Design for B.E. Partime - first semester – Computer Science and Engineering – Regulation 2014)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert 1128_{16} to decimal.
2. Represent a OR gate using NAND gate.
3. How a full adder is obtained from two half adders?
4. Convert the binary code 11101_2 to its equivalent grey code.
5. Differentiate a latch and a flipflop.
6. Draw the block diagram of a 4 bit serial in serial out right shift register.
7. Give an example for race free state assignment.
8. When asynchronous sequential circuits are preferred in circuits design.
9. Differentiate a SRAM and a DRAM.
10. What is a PLA in digital circuit?

PART B — (5 × 16 = 80 marks)

11. (a) Simplify the following using Quine-McCluskey method

$$f(A,B,C,D) = \sum m(0,2,8,10,12,13,14,15) + \sum d(5,7) \quad (16)$$

Or

(b) Implement a full adder using NOR gates only. (16)

12. (a) Explain carry lookahead adder with logic diagram. (16)

Or

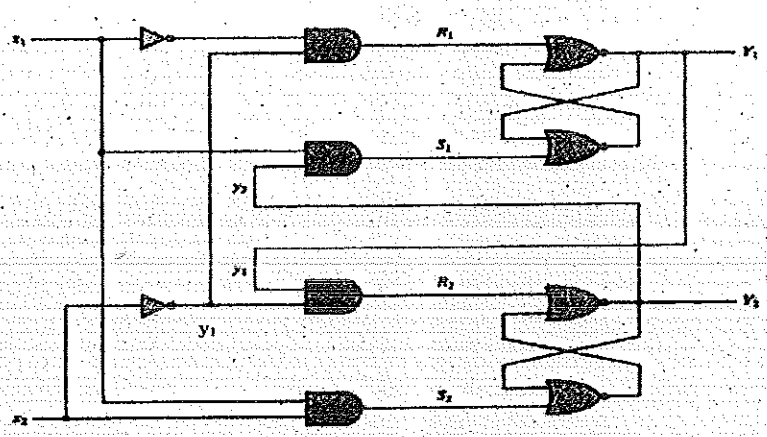
(b) Design and implement a gray to binary code converter (16)

13. (a) Design mod-10 synchronous counter using JK Flip Flops. (16)

Or

(b) With logic diagram explain the universal shift register as a storage device. (16)

14. (a) Analyse the given asynchronous sequential circuit (16)



Or

(b) Discuss in detail the race free state assignment with examples. (16)

15. (a) Explain

(i) RAM (8)

(ii) ROM (8)

Or

(b) Implement the combinational circuit having the shown truth table, using PLA. (16)

A	B	C	F1	F2
0	0	0	1	1
0	0	1	1	0
0	1	0	1	0
0	1	1	0	0
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	0	1