Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 91390

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2019

Second Semester

Computer Science and Engineering

CS 6201 – DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Information Technology)

(Regulations 2013)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A (10×2=20 Marks)

1. Classify the logic families by its operations.
2. State and prove the De Morgans' theorem.
3. Define Combinational circuits.
4. Design the combinational circuit with 3 inputs and 1 output. The output is 1 when the binary value of the inputs is less than 3. The output is 0 otherwise.
5. What is synchronous counter ?
6. Give the comparison between combinational circuits and sequential circuits.
7. Compare asynchronous and synchronous sequential circuit.
8. What is a critical race condition ? Give example.
9. What is memory address register ?
10. Write short notes on PLA.

PART – B (5×16=80 Marks)

11. a) i) Simplify the following Boolean expression to a minimum number of literals. (8)
A'B' + A'C'D' + A'B'D + A'B'CD'.

ii) Convert the given expression in canonical SOP form Y = AC + AB + BC. (8)

(OR)

b) i) List out the procedure for converting Binary to Gray Code. **(4)**

ii) Convert the following number from one base to other $(65.342)_8 = (\ )_7$. **(8)**

iii) What are the different ways to represent a negative number ? **(4)**

12. a) Design a full subtractor and derive expression for difference and borrow. Realize the circuit using gates. **(16)**

(OR)

b) Design a code converter that converts a 8421 to BCD code. Realize the circuits using gates. **(16)**

13. a) Implement the following Boolean function with a 4 × 1 multiplexer and external gates. Connect inputs A and B to the selection lines. The input requirements for the four data lines will be a function of variables C and D these values are obtained by expressing F as a function of C and D for each of the four cases when AB = 00, 01, 10 and 11. These functions may have to be implemented with external gates. $F(A, B, C, D) = \Sigma (1, 2, 5, 7, 8, 10, 11, 13, 15)$. **(16)**

(OR)

b) Draw a neat sketch showing implementation of $Z_1 = ab'd'e + a'b'c'e + bc + de$, $Z_2 = a'c'e$, $Z_3 = bc + de + c'd'e + bd$ and $Z_4 = a'c'e + ce$ using a 5*8*4 PLA. **(16)**

14. a) Summarize the design procedure for asynchronous sequential circuit. Give an illustration of it with a classical example. **(16)**

(OR)

b) Explain the different types of hazards that occurs in asynchronous sequential circuits and Combinational circuits. **(16)**

15. a) i) Write short notes on Address multiplexing. **(8)**

ii) Briefly discuss the sequential programmable devices. **(8)**

(OR)

b) i) Implement the following two Boolean functions with a PLA. **(10)**

F1 = A B′ + A C + A′ B C′

F2 = (AC + BC)′

ii) Give the Internal block diagram of 4 ×4 RAM. **(6)**