Reg. No. : | | | | | | | | | | | | |

Question Paper Code : X 20389

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2020
Second Semester
Computer Science and Engineering
CS 6201 – DIGITAL PRINCIPLES AND SYSTEM DESIGN
(Common to Information Technology)
(Regulations 2013)
(Common to PTCS 6201 – Digital Principles and System Design for B.E. (Part-Time) – Computer Science and Engineering – First Semester (Regulations 2014))

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. Convert $(126)_{10}$ to octal number and binary number.
2. Write short notes on weighted binary codes.
3. Implement a full adder with 4 × 1 Multiplexer.
4. Write the Data flow description of a 4-bit Comparator.
5. State the excitation table of JK-Flip Flop.
6. A seven bit Hamming code is received as 1111110. What is the correct code ?
7. When do race conditions occur ?
8. Define merger graph.
9. List the major differences between PLA and PAL.
10. What is memory decoding ?

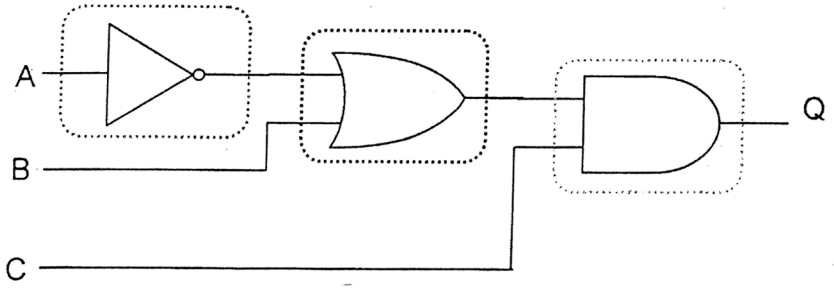
PART – B **(5×16=80 Marks)**

11. a) Simplify the following Boolean expression in
    i) Sum-of-product
    ii) Product-of-sum using Karnaugh map
    AC′ + B′D + A′CD + ABCD **(16)**

(OR)

b) i) Express the following function in sum of min-terms and product of max-terms :
$F(x, y, z) = x + yz$. **(8)**

ii) Convert the following logic system into NAND gates only. **(8)**



12. a) Design a full adder with inputs x, y, z and two outputs S and C. The circuits performs x + y + z, z is the input carry, C is the output carry and S is the sum. **(16)**

(OR)

b) Design a logic circuit that accepts a 4-bit Grey Code and convert it into 4-bit binary code. **(16)**

13. a) Design a sequence detector that detects a sequence of three or more consecutive 1's in a string of bits coming through an input line and produces an output whenever this sequence is detected. **(16)**

(OR)

b) Design a three bit synchronous counter with T flip flop and draw the diagram. **(16)**

14. a) Explain the analysis and design procedures of synchronous sequential circuits. **(16)**

(OR)

b) With necessary example and diagram, explain the concept of reduction of state and flow tables. **(16)**

15. a) Design a 16 bit RAM array (4 × 4 RAM) and explain the operation. **(16)**

(OR)

b) Explain the following :

i) ASIC **(8)**

ii) Field Programmable Gate Array. **(8)**