Reg. No. :

Question Paper Code : X20393

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2020
AND APRIL/MAY 2021
Third/Fifth/Sixth Semester
Computer Science and Engineering
CS 6303 – COMPUTER ARCHITECTURE
(Common to Information Technology, Electronics and Communication Engineering, Electronics and Instrumentation Engineering, Instrumentation and Control Engineering, Robotics and Automation Engineering)
(Regulations 2013)
(Also Common to PTCS 6303 – Computer Architecture for B.E. Part-Time – Second Semester/Third Semester for Computer Science and Engineering, Electronics and Communication Engineering – Regulations 2014)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. List the eight great ideas invented by computer architects.
2. Distinguish Pipelining from Parallelism.
3. What is a guard bit and what are the ways to truncate the guard bits ?
4. What is arithmetic overflow ?
5. Name the control signals required to perform arithmetic operations.
6. Define hazard. Give an example for data hazard.
7. State the need for Instruction Level parallelism.
8. What is Fine grained multithreading ?
9. How to avoid hazards ?
10. What is the difference between DLP and TLP ?

PART – B **(5×13=65 Marks)**

11. a) Explain in detail the various components of computer system with neat diagram.

(OR)

b) Explain the different types of Addressing modes with suitable examples.

12. a) i) Demonstrate multiplication of two binary numbers with an example. Design an arithmetic element to perform this multiplication. **(7)**

ii) Describe non restoring division with an example. **(6)**

(OR)

b) i) Design an arithmetic element to perform the basic floating point operations. **(7)**

ii) What is meant by sub word parallelism ? Explain. **(6)**

13. a) Explain the different types of pipeline hazards with suitable examples.

(OR)

b) Explain in detail how exceptions are handled in MIPS architecture.

14. a) Explain in detail about Flynn's classification.

(OR)

b) Write short notes on :

i) Hardware multithreading **(6)**

ii) Multicore processors. **(7)**

15. a) Explain in detail about cache performance evaluation and enhancement.

(OR)

b) Discuss in detail about virtual memory with suitable diagram.

PART – C **(1×15=15 Marks)**

16. a) What is the disadvantage of Ripple carry addition and how it is overcome in carry look ahead adder and draw the logic circuit CLA ?

(OR)

b) Design and explain a parallel priority interrupt hardware for a system with eight interrupt sources.

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