Question Paper Code : 70380

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2021.

Third / Fifth / Sixth Semester

Electronics and Communication Engineering

CS 6303 — COMPUTER ARCHITECTURE

(Common to Information Technology and Computer Science and Engineering / Electronics and Instrumentation Engineering/Instrumentation Control Engineering/ Robotics and Automation Engineering)

(Regulation 2013)

(Also Common to PTCS 6303 — Computer Architecture for B.E. (Part-Time) – Fifth Semester/ Second Semester – Electronics and Communication Engineering / Computer Science and Engineering (Regulations – 2014))

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is an instruction register?

2. Give the formula for CPU execution time for a program.

3. How overflow occur in subtraction?

4. What do you mean by sub word parallelism?

5. What is Flynn's taxonomy?

6. Define von Neumann architecture.

7. What is instruction level parallelism?

8. Distinguish implicit multithreading and explicit multithreading.

9. Define Memory hierarchy.

10. State the advantages of virtual memory.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Do the following changes to a computer system increase throughput, decrease response time, or both.

(1) Replacing the processor in a computer with a faster version

(2) Adding additional processors to a system that uses multiple processors for separate tasks-for example, searching the web.

Derive the performance matrics for the mentioned scenario. (7)

(ii) Discuss about power wall in computer architecture. (6)

Or

(b) (i) Write a short notes about logical operations. (7)

(ii) Give example to the various types of instruction operators. (6)

12. (a) Explain Booth's Algorithm for the multiplication of signed two's complement numbers.

Or

(b) Discuss in detail about division algorithm in detail with diagram and examples.

13. (a) What is pipelining? Discuss about pipelined data path and control. (13)

Or

(b) Briefly explain about various categories of hazards with examples. (13)

14. (a) (i) Discuss the challenges in parallel processing with necessary examples. (6)

(ii) Explain Flynn's classification of parallel processing with necessary diagrams. (7)

Or

(b) Explain the four principal approaches to multithreading with necessary diagrams. (13)

15. (a) Elaborate on the various memory technologies and its relevance. (13)

Or

(b) What is virtual memory? Explain the steps involved in virtual memory address translation. (13)

PART C — (1 × 15 = 15 marks)

16. (a) (i) Consider web browsing application. Assuming both client and server are involved in the process of web browsing application, where can caches be placed to speed up the process? Design a memory hierarchy for the system. Show the typical size and latency at various levels of the hierarchy. What is the relationship between cache size and its access latency? What are the units of data transfers between hierarchies? What is the relationship between the data location, data size, and transfer latency? (8)

(ii) The following sequence of instructions are executed in the basic 5-stage pipelined processor : (7)

```
lw $1, 40($6)
add $6, $2, $2
sw $6, 50($1)
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Indicate dependences and their type. Assuming there is no forwarding in this pipelined processor, indicate hazards and add NOP instructions to eliminate them.

Or

(b) Compare hardwired and microprogrammed control unit designs in terms of their mechanism of generating control signals with diagram. (15)

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