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Question Paper Code : 80289

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2016.

Sixth Semester

Electronics and Communication Engineering

CS 6303 — COMPUTER ARCHITECTURE

(Common to Third Semester Information Technology and Computer Science and Engineering)

(Regulations 2013)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is an instruction register?
2. Give the formula for CPU execution time for a program.
3. What is a guard bit and what are the ways to truncate the guard bits?
4. What is arithmetic overflow?
5. What is meant by pipeline bubble?
6. What is a data path?
7. What is instruction level parallelism?
8. What is multithreading?
9. What is meant by address mapping?
10. What is cache memory?

PART B — (5 × 13 = 65 marks)

11. (a) Explain in detail the various components of computer system with neat diagram.

Or

- (b) Explain the different types of Addressing modes with suitable examples.
12. (a) Explain Booth's Algorithm for the multiplication of signed two's complement numbers.

Or

- (b) Discuss in detail about division algorithm in detail with diagram and examples.
13. (a) Why is branch prediction algorithm needed? Differentiate between the static and dynamic techniques.

Or

- (b) Explain how the instruction pipeline works. What are the various situations where an instruction pipeline can stall?
14. (a) Explain in detail about Flynn's classification of parallel hardware.

Or

- (b) Discuss Shared memory multiprocessor with a neat diagram.
15. (a) Discuss DMA controller with block diagram.

Or

- (b) Discuss the steps involved in the address translation of virtual memory with necessary block diagram.

PART C — (1 × 15 = 15 marks)

16. (a) What is the disadvantage of Ripple carry addition and how it is overcome in carry look ahead adder and draw the logic circuit CLA.

Or

- (b) Design and explain a parallel priority interrupt hardware for a system with eight interrupt sources.