Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 31239

13.5.13-F

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2013.

Sixth Semester

Electrical and Electronics Engineering

080280056 – COMPUTER ARCHITECTURE

(Regulation 2008)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is a zero address instruction?

2. Differentiate arithmetic and logic micro-operations.

3. Give the use of MicroProgram Counter.

4. List the different types of addressing modes.

5. What are the fules for mul /div of floating point number?

6. State different types of hazards that can occur in pipeline.

7. What is the use of IO controller?

8. What are the advantages and disadvantages of bus?

9. How can the performance of a memory be measured?

10. Define memory access and memory cycle time.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain the basic functional units of a simple computer. (10)

(ii) Write in detail about error detecting codes. (6)

Or

(b) Write short notes on the following

(i) Timing and control cycle (6)

(ii) Register and Memory transfer. (5)

(iii) Fixed and floating point representation. (5)

12. (a) With a neat block diagram, explain in detail about micro programmed control unit and explain its operations. (16)

Or

(b) What are the types of instructions available in a system? With appropriate example explain the different addressing modes. (16)

13. (a) Give an algorithm to find the product of two signed binary numbers. Explain the necessary steps with example. (16)

Or

(b) Describe the basic structure of the pipeline processor and explain how it is carried out in floating point adder. (16)

14. (a) (i) Discuss the DMA driven data transfer technique. (8)

(ii) Describe the operation of any two input devices with diagram (8)

Or

(b) (i) What is the importance of I/O interface? Compare the features of SCSI and PCI Interfaces. (8)

(ii) Why is priority handling desired in interrupt controllers? How does the different priority scheme work? (8)

15. (a) (i) What are the various mapping techniques used in cache memories? Explain. (8)

(ii) Give the structure of semiconductor ROM memories. Explain read and write operation. (8)

Or

(b) Explain the virtual memory address translation and TLB with necessary diagram. (16)
