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16.5 FN

Question Paper Code : 73379

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2017.

Third/Fourth Semester

Computer Science and Engineering

CS 2253/10144 CS 404/CS 43/080250011/CS 1252 A — COMPUTER ORGANIZATION AND ARCHITECTURE

(Common to Information Technology)

(Regulations 2008/2010)

(Also Common to PTCS 2253 – Computer Organization and Architecture for B.E. (Part-Time) Third Semester – CSE – Regulations 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is meant by addressing mode? Mention its importance.

2. What is CISC? Mention its advantages.

3. What is the advantage of multibus organization?

4. List the advantages of register transfer.

5. Define structural hazard.

6. Give the features of the addressing mode suitable for pipelining.

7. Compare Static RAM and Dynamic RAM.

8. Define the terms hit, miss and ratio with respect to cache.

9. Distinguish between isolated and memory-mapped I/O.

10. Mention the advantages of USB.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain the working of a floating point adder/subtractor. Explain how floating point addition/subtraction is performed. (10)

(ii) Write a note on instruction set architecture. (6)

Or

(b) (i) Explain the representation of floating point numbers in detail. (8)

(ii) Explain various addressing modes with examples. (8)

12. (a) Write an explain the steps involved in the execution of a complete instruction. (16)

Or

(b) Explain the control signal generation using hardwired and microprogrammed control with necessary block diagrams. (16)

13. (a) (i) Describe the data and control path techniques in pipelining. (10)

(ii) Briefly explain the speedup performance models for pipelining. (6)

Or

(b) (i) What is instruction hazard? Explain in detail how to handle the instruction hazards in pipelining with relevant examples. (10)

(ii) Write note on exception handling. (6)

14. (a) Explain in detail about the principles of associative memories. (16)

Or

(b) Explain the features of cache memory and its mapping methods. How can its performance be improved? (16)

15. (a) Explain the following :

(i) Interrupts (10)

(ii) Buses. (6)

Or

(b) (i) Discuss about standard I/O interfaces. (8)

(ii) Discuss about PCI buses. (8)

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