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Question Paper Code : 51454

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2016

Fifth Semester

Electronics and Communication Engineering

EC 2303/EC 53/10144 EC 605 – COMPUTER ARCHITECTURE AND ORGANIZATION

(Common to Sixth Semester Biomedical Engineering)

(Regulations 2008/2010)

(Common to PTEC 2303 – Computer Architecture and Organization for B.E. (Part-Time) Fourth Semester, Electronics and Communication Engineering Regulations 2009)

Time : Three Hours **Maximum : 100 Marks**

Answer ALL questions.

PART – A (10 × 2 = 20 Marks)

1. What is a bus ? What are the different buses in a CPU ?
2. Define PC relative and Base Relative addressing mode.
3. Add (+7) with (–3) in binary.
4. Subtract (–5) from (–7) in binary.
5. What is cache memory ?
6. Define Associative memory.
7. Comment on locality reference.
8. What is memory address map ?
9. Differentiate between RISC and CISC architecture.
10. Why does DMA have priority over the CPU when both request a memory transfer ?

PART – B (5 × 16 = 80 marks)

11. (a) Explain the following addressing modes with an example and suggest the uses of those addressing modes : **(16)**

(i) Register Indirect

(ii) Auto increment

(iii) Indirect addressing

(iv) Base addressing

(v) Indexed addressing.

OR

(b) Explain in detail about the Accumulator based CPU organization with a neat block diagram. **(16)**

12. (a) Draw and explain the block diagram used to perform carry look ahead addition with the necessary equations. **(16)**

OR

(b) Divide 21 (twenty one) by 3 (three) using non-restoring method and explain the steps involved, with the neat diagram. **(16)**

13. (a) Explain with relevant diagrams, the design of microprogrammed control unit. **(16)**

OR

(b) Explain with flow chart, the instruction pipelining. **(16)**

14. (a) Explain how multiplication is carried out using Booth's algorithm. Extend it for floating point operation. What are the advantages of modified Booth's algorithm ?

OR

(b) What is look ahead carry addition ? How to design combinational and sequential ALUs to handle computation on arithmetic and logic data ?

15. (a) (i) Design a parallel priority interrupt hardware for a system with eight interrupt sources. **(8)**

(ii) What are handshaking signals ? Explain asynchronous data transfer using handshake signals. **(8)**

OR

(b) (i) What is bus arbitration ? Describel the centralized approach for bus arbitration with the help of diagram. **(8)**

(ii) Describe the architecture of a typical superscalar processor with the help of a block diagram. **(8)**
