Reg. No. :

Question Paper Code : 31363

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2013.

Fifth Semester

Electronics and Communication Engineering

EC 2303/EC 53/10144 EC 605 — COMPUTER ARCHITECTURE AND ORGANIZATION

(Common to Sixth Semester Biomedical Engineering)

(Regulation 2008/2010)

(Common to PTEC 2303 – Computer Architecture and Organization for B.E. (Part-Time) Fourth Semester, Electronics and Communication Engineering, Regulation 2009)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — $(10 \times 2 = 20 \text{ marks})$

- 1. Write the general format for floating-point numbers.
- 2. What information is provided by the addressing modes?
- 3. How overflow is detected in fixed point arithmetic?
- 4. What is the difference between restoring and non-restoring division algorithms?
- 5. What is pipelining?
- 6. What is microinstruction and microprogram?
- 7. What is cache memory?
- 8. What is memory address map?
- 9. List the important characteristics of RISC.
- 10. Explain the term handshaking related to data transfer.

- PART B $(5 \times 16 = 80 \text{ marks})$
- 11. (a) What are the different types of CPU organization? Explain with relevant diagrams. (16)

Or

- (b) (i) With examples explain the different types of instruction formats. (6)
 - (ii) Explain the different types of Addressing modes with suitable examples. (10)
- 12. (a) With flow chart and numerical example explain Booth's multiplication algorithm. (16)

Or

- (b) With relevant diagram and expressions, explain the operation of carry look ahead adder. (16)
- 13. (a) Explain with relevant diagrams, the design of microprogrammed control unit. (16)

Or

(b)	Explain with flow chart, the instruction pipelining.	
4. (a)	With relevant block diagrams, explain the concept of	
	(i) Associative memory	(8)
	(ii) Virtual memory.	(8)

Or

(b)	Wri	Write notes on		
a	(i)	Magnetic memories	(8)	
	(ii)	Optical memories.	(8)	

15. (a) Explain the IOP organization and communication between CPU and IOP. (16)

Or

(b) With block diagrams, explain data transfer using DMA controller. (16)