Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 51343

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2014.

Fourth Semester

Computer Science and Engineering

CS 2253/CS 43/CS 1252 A /080250011/10144 CS 404 — COMPUTER ORGANIZATION AND ARCHITECTURE

(Common to Information Technology)

(Regulation 2008/2010)

(Also Common to PTCS 2253–Computer Organisation and Architecture for B.E. (Part–Time) Third Semester – CSE –Regulation 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. State the basic performance equation.
2. What do you mean by an interrupt?
3. Define data path.
4. What do you mean by data control stores?
5. Define structural hazard.
6. Give the features of the addressing mode suitable for pipelining.
7. What do you mean by locality of reference?
8. Define Supervisor state.
9. Define memory mapped Input / Output.
10. What is the advantage of DMA?

PART B — (5 × 16 = 80 marks)

11. (a) What do you mean by addressing modes? Explain the types of addressing modes that exists in modern processors? (16)

Or

(b) (i) Explain the rules for basic arithmetic operations of floating point numbers? (10)

(ii) Explain Guard bit and Truncation? (6)

12. (a) (i) Explain in detail the control sequence for an unbranch instruction, unconditional and conditional branch instruction. (12)

(ii) Give the control sequence for the instruction Add R4,R5,R6. (4)

Or

(b) Discuss hardwired control in detail. (16)

13. (a) Explain data hazard in detail. (16)

Or

(b) Discuss the methods to reduce hazards due to conditional branches. (16)

14. (a) Explain, in detail, the principles of associative memories. (16)

Or

(b) Explain the features of cache memory and its accessing. How can its performance be improved? (16)

15. (a) Discuss Direct Memory Access in detail. (16)

Or

(b) Define plug and play and Explain SCSI in detail. (16)

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