Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 13704

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2012.

Fourth Semester

Computer Science and Engineering

080250011 — COMPUTER ORGANIZATION AND ARCHITECTURE

(Common to Information Technology)

(Regulation 2008)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Compare single bus structure and multiple bus structure.
2. What is multitasking?
3. Define data path.
4. What is micro programmed control?
5. List the basic steps in pipelining.
6. What is structural hazard?
7. Define Memory Latency.
8. Define miss penalty.
9. What is cycle stealing?
10. List the functions of I/O interface.

PART B — (5 × 16 = 80 marks)

11. (a) Explain various addressing modes.

Or

(b) Enumerate ALU design.

12. (a) Describe the Execution of a complete instruction.

Or

(b) Explain the concept of micro programmed control unit.

13. (a) Explain instruction hazards.

Or

(b) Describe exception handling and data path considerations.

14. (a) Describe Memory Interleaving and the addressing of multiple modules Memory system.

Or

(b) Explain virtual memory implementation using paging.

15. (a) Describe about PCI, SCSI.

Or

(b) Explain Direct Memory Access.
