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Question Paper Code : 91357

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2014.

Sixth Semester

Computer Science and Engineering

CS 2354/CS 64/10144 CS 604 — ADVANCED COMPUTER ARCHITECTURE

(Regulation 2008/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is the major limitation of pipeline techniques?

2. How many branch-selected entries are in a (2, 2) branch predictor that has a total of 8K bits in prediction buffer.

3. List down the issues in the design of simultaneous multithreaded processors.

4. What is the key feature in the microarchitecture of Itanium2.

5. What do you mean by Multithreading?

6. Define sequential consistency.

7. Suppose you want to achieve a speedup of 80 with 100 processors. What fraction of the original computation can be sequential?

8. Define transaction time.

9. What do you mean by hyperthreading?

10. Define SMT.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Consider the following measurements :

Frequency of FP operations (other than FPSQR) = 25%

Average CPI of FP operations = 4.0

Average CPI of other instructions = 1.33

Frequency of FPSQR = 2%

CPI of FPSQR = 20

Assume that two design alternatives are to decrease the CPI of FPSQR to 2 or to decrease the average CPI of all FP operations to 2.5. Compare these two design alternatives using the CPU performance Equation. (8)

(ii) Describe the types of optimizations performed by the modern compilers. (8)

Or

(b) (i) Using Tomasulo's Algorithm, Show the information tables for the following code sequence.

```
Loop :  L.D      F0, 0(R1)
        MUL.D    F4, F0, F2
        S.D      F4, 0(R1)
        DADDUI   R1, R1, –8
        BNE      R1, R2, Loop;
```

Assume all the instructions were issued in two successive iterations of the loop, but none of the floating-point load-stores or operations has completed. (8)

(ii) Explain the various dynamic branch prediction schemes. (8)

12. (a) (i) Explain the methods of exploiting ILP using VLIW processor. (8)

(ii) Describe the register naming approach for implementation of speculation. (8)

Or

(b) (i) Compare the hardware Vs software speculation mechanisms. (10)

(ii) What are the important limitations to ILP? (6)

13. (a) Explain the models of memory consistency in multiprocessor system. (16)

Or

(b) Explain the snoopy cache coherence protocol for ensuring coherence in symmetric multiprocessors. (16)

14. (a) Explain the categories of misses and how will you reduce cache miss rate. (16)

Or

(b) (i) Explain the steps in designing an I/O system. (8)

(ii) Write a short note on fault, failures and errors. (8)

15. (a) Explain the SUN CMP architecture. (16)

Or

(b) Discuss the design issues and implementation of Intel Multicore architectures. (16)
