Reg. No. :		T	
neg. No.:			

Question Paper Code: 73391

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2017.

Sixth Semester

Computer Science and Engineering

CS 2354/CS 64/10144 CS 604 — ADVANCED COMPUTER ARCHITECTURE

(Regulations 2008/2010)

Time: Three hours

Maximum: 100 marks

Answer ALL questions.

PART A — $(10 \times 2 = 20 \text{ marks})$

- 1. Define temporal and spatial locality.
- 2. What are the major advantages of dynamic scheduling using Tomasulo's approach?
- 3. List any five primary characteristics of EPIC multiple issue processor.
- 4. What are the limitations of multiple issue processor?
- 5. What are the disadvantages of using symmetric shared memory?
- 6. What is consistency?
- 7. Point out how RAID can improve the performance of I/O.
- 8. What is the need to implement memory as a hierarchy?
- 9. What is multicore?
- 10. What are the design issues of cell processor?

PART B — $(5 \times 16 = 80 \text{ marks})$

11. (a) What is instruction-level parallelism? Explain in detail about the various dependences caused in ILP.

Or

(b) Explain how to reduce branch cost with dynamic hardware prediction.

2. (a)		(i)	Briefly compare CISC, RISC and VLIW.	(6)			
		(ii)	Describe the architecture of a typical superecalar VLIW procues with the help of block diagram.	essor (10)			
			\mathbf{Or}				
	(b)	(i)	Describe the basic compiler techniques for exploiting instru- level parallelism.	(10)			
		(ii)	Briefly compare hardware and software speculation mechan	isms. (6)			
3.	(a)	Discuss in detail about the performance issues in symmetric and distributed shared memory architectures.					
			Or	3			
	(b)	What is the need of memory consistency model? Explain its types.					
4.	(a)	Discuss the various cache Optimization techniques. (16)					
			Or				
	(b)	(i)	Briefly describe the various RAID levels.	(8)			
		(ii)	Explain the steps in designing an I/O system.	(8)			
5.	(a)	(i)	Discuss the design challenges of SMT architecture.	(8)			
		(ii)	Explain the Intel multicore architecture with its benefits.	(8)			
			Or				
	(b)	(i)	Explain in detail about the CMP architecture and its perform	ance. (8)			
4		(ii)	Explain the architecture of IBM cell processor with neat diagram.	block (8)			

2 73391