Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 52387

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2017
Sixth Semester
Computer Science and Engineering
CS 2354 : ADVANCED COMPUTER ARCHITECTURE
(Regulations 2008)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. Define control dependency. Give an example.
2. Mention the advantage of using tournament based predictors.
3. What are the types of multiple issue processors ?
4. What is the limitation of VLIW processors ?
5. What happens when a private and shared item is cached ?
6. What are the disadvantages of using symmetric shared memory ?
7. How to calculate average memory access time with 2 and 4-way ?
8. What is JBOD ?
9. List out the advantages of heterogeneous multicore processors.
10. State fine grained multi-threading.

PART – B **(5×16=80 Marks)**

11. a) Illustrate in detail the technique used for overcoming data hazards. **(16)**

(OR)

b) i) Explain the basic compiler techniques for exposing ILP. **(8+8)**

ii) Show how the following loop would look on MIPS, both scheduled and unscheduled including any stalls.

for (i = 1000; i > 0; i = i – 1)

x[i] = x[i] + s;

12. a) Explain hardware support for compilers for exposing ILP. (16)

(OR)

b) i) Explain Intel IA-64 architecture in detail with suitable references to Itanium processor.

ii) Explain the limitations of ILP. (8+8)

13. a) Explain the symmetric shared memory architecture. Explain the snooping based protocols with neat diagram. (16)

(OR)

b) i) Explain how multithreading approach can be used to exploit thread level parallelism within a processor.

ii) Describe how to implement synchronization using locks and unlocks in Multiprocessor. (8+8)

14. a) Explain in detail about the various optimization techniques for improving the cache performance. (16)

(OR)

b) i) Describe in detail about redundant array of inexpensive disks (RAID).

ii) Explain in detail about buses and bus design decisions. (8+8)

15. a) i) Explain in detail about the various types of software and hardware based multi-threading. (8)

ii) Explain simultaneous multi-threading concept for converting thread level parallelism into instruction level parallelism. (8)

(OR)

b) i) Describe Intel multi core architecture in detail.

ii) Explain the architectural features of IBM cell processors with neat diagram. (8+8)