Reg. No. :

Question Paper Code : X 60390

B.E./B.Tech. DEGREE EXAMINATIONS, NOV./DEC. 2020
Sixth Semester
Computer Science and Engineering
CS 2354/CS 64/10144 CS 604 – ADVANCED COMPUTER ARCHITECTURE
(Regulations 2008/2010)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. Define Dynamic scheduling.
2. List the five levels of branch prediction.
3. What are the advantages of superblock approach ?
4. What are the functional units of Itanium processor ?
5. What is loop unrolling and what are the major limitation of loop unrolling ?
6. What is multiprocessor cache coherence problem ?
7. A certain memory configuration has four levels M_1, M_2, M_3 and M_4 with hit ratios of 0.7, 0.85, 0.97, 1.0 respectively. A program P makes 3000 references to this memory system. Calculate the exact number of references Ri made by P to each level of memory, Mi.
8. Compare static and dynamic RAM.
9. Enlist the features of SMT Architecture.
10. Point out the advantages and disadvantages of heterogeneous multi-core processors.

PART – B **(5×16=80 Marks)**

11. a) Explain how compiler technology can be used to enhance a processor's ability to exploit ILP.

(OR)

b) What are the different ways for branch prediction ? Discuss how pipeline performance issues can be reduced by branch prediction.

12. a) Explain the VLIW approach with example. **(16)**

(OR)

b) i) Give the limitations of ILP. **(6)**

ii) Discuss the major advantages and disadvantages of supporting speculation in software and hardware. **(10)**

13. a) i) What do you mean by snooping protocol ? Explain how it is used to maintain the coherence. **(8)**

ii) Explain the different models of memory consistency. **(8)**

(OR)

b) i) Discuss the directory based cache coherence protocol. **(8)**

ii) Explain how the hardware primitives can be used to build synchronization operations. **(8)**

14. a) Describe various techniques for optimization of cache in detail. **(16)**

(OR)

b) i) Briefly describe standard RAID levels in detail. **(10)**

ii) Discuss about the issues in designing I/O system. **(6)**

15. a) How is multithreading used to exploit thread level parallelism within a processor ? Explain with example.

(OR)

b) Discuss SMT and CMP architectures in detail.

———————