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Question Paper Code : 80094

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2019.

Third Semester

Computer Science and Engineering

CS 8351 – DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Electronics and Telecommunication Engineering/Information Technology)

(Regulation 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Represent 3856 in BCD and 2421 code.

2. Simplify the following Boolean function.

   $F = x'y' + xy + x'y$.

3. Construct a full adder using two half adders and OR gate.

4. Write the truth table of 2 to 4 line decoder and draw its logic diagram.

5. State the difference between latches and flipflops.

6. What is meant by edge triggered flip flops?

7. Draw the logic diagram and write the function table of D Latch.

8. What is meant by race free condition in sequential circuits?

9. What are error detecting codes? Give examples.

10. List the advantages of using sequential programmable devices.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Convert the following numbers to decimal

$(11011.101)_2, (5432)_6$. (4)

(ii) Perform the following arithmetic operation using 2's complement arithmetic.

$(11011100)_2 - (10011011)_2$. (3)

(iii) Express the following functions in sum of minterms and product of maxterms.

$F(ABCD) = A'B + BD + AC'$. (6)

Or

(b) (i) Demonstrate by means of truth tables the validity of the DeMorgan's theorem for three variables: (4)

$(XYZ)' = X' + Y' + Z'$

(ii) Simplify the following Boolean functions by means of a 4-variable map $F(A, B, C, D) = \sum m(0, 2, 4, 5, 8, 10, 14, 15)$. (5)

(iii) Implement the following Boolean function only with NAND gates, using a minimum number of gate inputs: $F(A, B, C, D) = AB + CD$. (4)

12. (a) (i) Design of 4 bit binary adder-subtractor circuit. (5)

(ii) Design a combinational circuit that accepts a 3-bit number and generates a 6-bit binary number output equal to the square of the input number. Write a high-level behavior VHDL description for the circuit. (8)

Or

(b) (i) Explain the Logic Diagram of a 4-Input Priority Encoder. (8)

(ii) Implement the following Boolean function with an 8–to–1–line multiplexer and an inverter. $F(A, B, C, D) = \sum (2, 4, 6, 9, 10, 11, 15)$. (5)

13. (a) (i) Describe the operations of R-S flip flop with a neat sketch. (5)

(ii) Design a sequential circuit with two D flip- flops A and B and one input X. When $X = 0$, the state of the circuit remains the same. When $X = 1$, the circuit goes through the state transitions from 00 to 10 to 11 to 01, back to 00 and then repeats. (8)

Or

(b) (i) Construct a clocked Master Slave J-K Flip flop and explain. (5)

(ii) A sequential circuit with two D flip- flops A and B, two inputs X and Y, and one output Z is specified by the following input equations: (8)

$A(t + 1) = x'y + xA$

$B(t + 1) = x'B + xA$

$z = B$

Draw the logic diagram of the circuit. Derive the state table and state diagram and state whether it is a Mealy or a Moore machine.

14. (a) (i) Write the difference between synchronous and asynchronous sequential circuit. (4)

(ii) Outline the procedure for analyzing asynchronous sequential circuit. (9)

Or

(b) (i) Discuss about the possible hazards and methods to avoid them in combinational circuits. (5)

(ii) Discuss about the possible hazards in sequential circuits. (8)

15. (a) (i) Discuss briefly about RAM and its types. (5)

(ii) Explain the logical construction of a 256 × 8 RAM using 64 × 8 RAM chips. (8)

Or

(b) (i) Given the 8 bit data word 10011010 generate the 13 bit composite word for the Hamming code that corrects single errors and detect double errors. (4)

(ii) Implement the following two Boolean functions with a PLA: (9)

$F1(A, B, C) = AB' + AC + A'BC'$

$F2(A, B, C) = (AC + BC)'$.

PART C — (1 × 15 = 15 marks)

16. (a) (i) Design a BCD to excess-3 code converter and explain. (8)

(ii) Draw and explain the logic circuit of a 4-bit magnitude comparator. (7)

Or

(b) (i) Explain the operations of a 4-bit bidirectional Shift Register. (8)

(ii) Write the VHDL code for a 4-bit binary –up counter and explain. (7)

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