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**Question Paper Code : 40387**

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2021.

Third Semester

Computer Science and Engineering

CS 8351 — DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Electronics and Telecommunication Engineering/  
Information Technology)

(Regulations 2017)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What are the basic digital logic gates?
2. Find the complement of the expression –  $(x + y' + z)(x' + z')(x + y)$ .
3. What is priority encoder?
4. List out the applications of multiplexer.
5. What is sequential circuit?
6. How many flip-flops are required to build a binary counter that counts from 0 to 1023?
7. Define hazard and when do hazard occur?
8. Define flow table in asynchronous sequential circuit.
9. List the major differences between PLA and PAL.
10. Differentiate volatile and non-volatile memory.

PART B — (5 × 13 = 65 marks)

11. (a) Express the following numbers in decimal
- (i)  $(10110.0101)_2$  (3)
  - (ii)  $(16.5)_{16}$  (3)
  - (iii)  $(26.24)_8$  (3)
  - (iv)  $(FAFA.B)_{16}$  (2)
  - (v)  $(1010.1010)_2$ . (2)

Or

- (b) Using K map, minimize the expression  
 $F(A, B, C, D) = \Sigma m(1, 3, 4, 6, 8, 9, 11, 13, 15) + \Sigma d(0, 2, 14)$ .

12. (a) Design a full adder and realize using gates. Implement full adder with two half adders and an OR gate.

Or

- (b) (i) Implement the Boolean expression  $F(A, B, C) = \Sigma m(0, 2, 5, 6)$  using 4 : 1 multiplexer. (7)
- (ii) Implement  $F(A, B, C, D) = \Sigma m(0, 1, 5, 6, 8, 10, 12, 15)$  using 8 : 1 multiplexer. (6)

13. (a) Show that the characteristic equation for the complement output of a JK flip-flop is  $Q'(t+1) = J'Q' + KQ$ .

Or

- (b) Design and implement a synchronous 4-bit up/down binary counter using T flip-flops.

14. (a) An asynchronous sequential circuit is described by the following excitation and output function,

$$Y = x_1 x_2 + (x_1 + x_2)y$$

$$Z = Y.$$

- (i) Draw the logic diagram of the circuit. (5)
- (ii) Derive the transition table, flow table and output map. (5)
- (iii) Describe the behavior of the circuit. (3)

Or

- (b) Explain with neat diagram about the static hazard and the way to eliminate it.

15. (a) A 12-bit Hamming code word containing 8 bit of data and 4 parity bits is read from memory. What was the original 8-bit data word that was written into memory if the 12 bit word read out is as follows?
- (i) 00001 110101 0 (4)
- (ii) 10111 00001 10 (4)
- (iii) 101111 110100 (5)

Or

- (b) Tabulate the PLA programming table for the four Boolean functions listed below. Minimize the numbers of product terms.

$$A(x, y, z) = \Sigma m(1, 2, 4, 6)$$

$$B(x, y, z) = \Sigma m(0, 1, 6, 7)$$

$$C(X, y, z) = \Sigma m(2, 6)$$

$$D(x, y, z) = \Sigma m(1, 2, 3, 5, 7)$$

PART C — (1 × 15 = 15 marks)

16. (a) Design an adder to perform arithmetic addition of two decimal digits in BCD.

Or

- (b) Design and write a HDL code for combinational circuits that's a four bit Binary code to four bit Gray code using Exclusive – OR gates.

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