Reg. No. : | | | | | | | | | | | | |

Question Paper Code : X 10315

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2020/
APRIL/MAY 2021
Fourth/Fifth/ Seventh Semester
Computer Science and Engineering
CS 8491 – COMPUTER ARCHITECTURE
(Common to Computer and Communication Engineering/Robotics and Automation/Information Technology)
(Regulations 2017)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. What are the various units in the computer ?
2. What is the absolute addressing mode ?
3. Draw the circuit diagram for half adder.
4. Show that the logic expression Cn ⊕ Cn – 1 is a correct indicator of overflow in the addition of 2's complement integers, by using an appropriate truth table.
5. What are the steps required for a pipelined processor to process the instruction ?
6. What is locality of reference ?
7. What are multiprocessors ? Mention the categories of multiprocessors.
8. What is NUMA processor ?
9. When is a memory unit called as RAM ?
10. Define vectored interrupts.

PART – B **(5×13=65 Marks)**

11. a) Explain the components of a computer with the block diagram in detail.

(OR)

b) What do you mean by addressing modes ? Explain various addressing modes with the help of examples.

12. a) Describe in detail Booth's multiplication algorithm and perform the Booth's operation for the 5-bit signed operand, +23 is the multiplicand, and its multiplied by –10, the multiplier to get the 10-bit product –230. Similarly find the remaining three combinations numbers. (+23 × + 10, –23 × – 10, –23 × –10).

(OR)

b) Write a non-restoring and restoring algorithm then perform the number 8/3 integer division using non-restoring division.

13. a) Describe in detail pipelined implementation of data path and control with diagrams.

(OR)

b) Find out the hazards in the following instructions and eliminate them by using stalls :

LW R_1, 0(R_2)
SUB R_4, R_1, R_5
AND R_6, R_1, R_7
OR R_8, R_1, R_9

14. a) Discuss the principle of hardware multithreading and elaborate its types.

(OR)

b) Explain about the multicore processors.

15. a) i) With neat sketch explain about Synchronous DRAMS. **(6)**

ii) With neat sketch explain about Asynchronous DRAMS. **(7)**

(OR)

b) Explain briefly about direct memory access.

PART – C **(1×15=15 Marks)**

16. a) Discuss the different mapping techniques used in cache memories and their relative merits and demerits.

(OR)

b) A computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte.

i) Calculate the number of bits in each of the Tag, Block and Word fields of the memory address. **(7)**

ii) If the cache is organized as a 2-way set associative cache that uses the LRU replacement algorithm. **(8)**

———————