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Question Paper Code : 66089

M.E./M.Tech. DEGREE EXAMINATION, DECEMBER 2015/JANUARY 2016

First Semester

Computer Science and Engineering

CP7103 : Multicore Architecture

(Common to M.Tech. Information Technology, M.E. Computer Science and Engineering (with Specialization in Networks) and M.E. Multimedia Technology)

(Regulations : 2013)

Time : Three Hours **Maximum : 100 Marks**

Answer ALL questions.

PART – A (10 × 2 = 20 Marks)

1. Define principle of locality and distinguish the different types of locality.

2. Some microprocessors today are designed to have adjustable voltage, so a 15% reduction in voltage may result in a 15% reduction in frequency. What would be the impact on dynamic energy and on dynamic power ?

3. List out any two usage of strides in vector architecture with a suitable example.

4. Use the GCD to determine whether dependences exist in the following loop :

```
for (i=0; i<100; i=i+l) {
    X[2*i+3] = X[2*i] * 5.0;
}
```

5. What is cache coherence ? How does it impact the consistency of a multi-processor system ?

6. Compare ILP, DLP, TLP and RLP.

7. What is the average memory latency of warehouse-scale computer assuming that 90% of accesses are local to the server, 9% are outside the server but within the rack and 1% are outside the rack but within the array ?

8. Distinguish the OPEX and CAPEX in measuring the cost of Warehouse-Scale Computer (WSC).

9. Identify the major elements of embedded system model.

10. Name any three challenges in designing an embedded system.

PART – B (5 × 13 = 65 Marks)

11. (a) (i) Explain the various terms involved in measuring, summarizing and reporting the performance of a computer system. **(7)**

(ii) How do you measure the processor performance ? Derive an equation to measure the performance of a processor. **(6)**

OR

(b) (i) How will you overcome data hazard with dynamic scheduling ? Give a suitable example. **(6)**

(ii) Briefly explain the dynamic scheduling using Tomasulo's approach. **(7)**

12. (a) (i) Suppose we have 8 memory banks with a bank busy time of 6 clocks and a total memory latency of 12 cycles. How long will it take to complete a 64-element vector load with a stride of 1 and with a stride of 32 ? **(7)**

(ii) Consider a loop like this one :

```
for (i=0; i<100; i=i+l) {
    A[i] = A[i] + B[i];      /* S1 */
    B[i+1] = C[i] + D[i];    /* S2 */
}
```

What are the dependences between S1 and S2 ? Is this loop parallel ? If not, show how to make it parallel ? **(6)**

OR

(b) Explain the basic structure of vector architecture with neat diagram. Give a suitable example to explain the working of vector processor. **(13)**

13. (a) Explain the snooping cache coherence protocol to implement the centralized shared memory architecture. Draw necessary diagrams. **(13)**

OR

(b) Explain the directory based cache coherence protocol to implement distributed shared memory architecture. **(13)**

14. (a) Explain the physical infrastructure, cost and measuring efficiency of a warehouse-scale computer. **(13)**

OR

(b) (i) Given that the costs of MapReduce jobs are growing and already exceed $100M per year, imagine that your boss wants you to investigate ways to lower costs. Two potentially lower cost options are either AWS Reserved Instances or AWS Spot Instances. Which would you recommend ? **(7)**

(ii) How long does it take to transfer 1000 MB between disks within the server, between servers in the rack, and between servers in different racks in the array ? How much faster is it to transfer 1000 MB between DRAM in the three cases ? (6)

15. (a) Explain the various stages in creating embedded system design. Draw an embedded system design and development life cycle model. (13)

OR

(b) Explain any five standards implemented in embedded system with its purpose. (13)

PART – C (1 × 15 = 15 Marks)

16. (a) Develop a case study on resource allocation in Warehouse-Scale Computers (WSCs) and Total Cost of Ownership (TCO). (15)

OR

(b) Design any one case study for an embedded system application such as consumer electronics, commercial office, automotive, aerospace and defence etc. (15)