Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 71187

M.E./M.Tech. DEGREE EXAMINATION, JUNE/JULY 2013.

First Semester

21.6.13-FN

Computer Science and Engineering

CS 9211/CS 911/10244 CS 105 — COMPUTER ARCHITECTURE

(Common to M.Tech. Information Technology)

(Regulation 2009/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. State Amdahl's law.

2. Consider the execution of a program of 15000 instruction by linear pipeline processor. The clock rate of pipeline is 25 MHz. Pipeline has five stages and one instruction is issued per clock cycle. Neglect penalties due to branch instructions and out of sequence execution. Calculate the speedup program execution by pipeline as compared with that by non-pipelined processor.

3. Differentiate spatial and temporal locality.

4. List out the difficulties that cause the instruction pipeline to deviate from its normal operation.

5. Mention the limitations of predicted instructions.

6. What is meant by poison bit?

7. How many branch selected entries are in a (2,2) predictors that has a total of 8k bits in a prediction buffer?

8. What are the steps to design an I/O System?

9. State Little's law.

10. What are the protocols to maintain coherence?

PART B — (5 × 16 = 80 marks)

11. (a) Explain with examples the various hazards in pipelining. (16)

Or

(b) (i) What is memory addressing and explain the different addressing modes in instruction set architecture? (6)

(ii) Discuss the main issues that arise when the vector length in a program in not exactly 64. (10)

12. (a) Explain in detail about tomasulo's algorithm, Discuss how does it overcome data hazard using dynamic scheduling with example.

Or

(b) (i) What is ILP? Discuss the limitations of ILP. (8)

(ii) Explain in detail about the various dependencies caused in ILP. (8)

13. (a) Give detailed explanation about the VLIW Approach.

Or

(b) (i) Explain how hardware support for exposing more parallelism at compile time. (8)

(ii) Differentiate hardware and software speculation mechanisms. (8)

14. (a) Explain snooping protocol with a state diagram.

Or

(b) (i) Discuss how multithreading is used to exploit thread level parallelism within a processor. (8)

(ii) Discuss the design challenges in SMT Processors. (8)

15. (a) (i) Explain the various Levels of RAID. (6)

(ii) Assume, a system where the clocks per instruction is 1.0 when all memory accesses hit in the cache. The only data accesses are loads and stores, and these total 50% of the instruction. If the miss penalty is 25 clock cycles and the miss rate is 2%, how much faster would the system be if all instructions were cache hits? (10)

Or

(b) (i) Explain different techniques to reduce cache miss penalty. (10)

(ii) To show equivalency between the two miss rate equations, assuming a miss rate per 1000 instructions of 30. Derive memory stall time in terms of instruction count. (6)
