Reg. No. : | | | | | | | | | | | | |

# Question Paper Code : 47115

M.E./M.Tech. DEGREE EXAMINATION, JANUARY 2018
First Semester
Computer Science and Engineering
CP5152 – ADVANCED COMPUTER ARCHITECTURE
(Common to M.E. Computer Science and Engineering (with Specialization in Networks)/ M.E. Multimedia Technology/M.Tech. Information Technology)
(Regulations 2017)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. List the challenges in exposing instruction level parallelism.
2. Differentiate coarse grained and fine grained multithreading.
3. When do we say that a cache block is exclusive ?
4. What happens when a private and shared items are cached ?
5. List the disadvantages of using symmetric shared memory.
6. What are the issues that occur with cache coherence ?
7. In what way is multicore processor superior to single core processor ?
8. Define the effectiveness of power utilization.
9. Highlight the improvements obtained with graphics processing units.
10. Compare scalar and vector processors.

PART – B **(5×13=65 Marks)**

11. a) Describe in details about the various dependences caused in ILP ? What are the limitations of ILP ? **(9+4)**

(OR)

b) Discuss how hardware based speculation is used to overcome control dependence. **(13)**

12. a) Describe the various cache hit time reduction techniques for improving the cache performance. **(13)**

(OR)

b) i) Elaborate on the technique for reducing cache miss penalty. **(8)**

ii) Explain segmented virtual memory protections with suitable example. **(5)**

13. a) Explain the distributed memory architecture with different message passing mechanisms. **(13)**

(OR)

b) i) Describe the implementation of directory-based cache coherence protocol. **(8)**

ii) How to implement synchronization of processes in a multiprocessor using hardware primitives ? **(5)**

14. a) i) With neat sketch explain the architectural features of IBM cell processor. **(7)**

ii) Compare SMT and CMP architectures. **(6)**

(OR)

b) i) State and explain the requirements and characteristics of warehouse scale computers. **(8)**

ii) Justify the term – "Return of utility computing". How it is related to WSC ? **(5)**

15. a) i) Describe the primary components of the instruction set architecture of VMIPS and explain the basic vector architecture with neat block diagram. **(8)**

ii) List any five double-precision floating-point VMIPS vector instructions and explain its functions. **(5)**

(OR)

b) Discuss the similarities and differences between the following :

i) Vector architectures and GPUs. **(7)**

ii) Multimedia SIMD computers and GPUs. **(6)**

PART – C **(1×15=15 Marks)**

16. a) i) Suppose we have an application running on a 32-processor multiprocessor, which has a 200 ns time to handle reference to a remote memory. For this application, assume that all the references except those involving communication hit in the local memory hierarchy, which is slightly optimistic. Processors are stalled on a remote request, and the processor clock rate is 3.3 GHz. If the base CPI (assuming that all references hit in the cache) is 0.5, how much faster is the multiprocessor if there is no communication versus if 0.2% of the instructions involve a remote communication reference ? **(7)**



ii) A 40 MHz processor was used to execute a benchmark program with the following instructions mix and clock cycle counts. **(8)**

| Instruction types | Instruction count | Clock cycle count |
|---|---|---|
| Integer arithmetic | 45000 | 1 |
| Data transfer | 32000 | 2 |
| Floating point | 15000 | 2 |
| Control Transfer | 8000 | 2 |

Determine the effective CPI, MIPS rate and execution time for this program. Give justification for each.

(OR)

b) i) A design choice is to be made in enhancing a processor. One option is to invest in additional hardware that works at twice the speed which will benefit 60% of the program. The other is to keep the hardware simple, but invest in compiler optimization, which provides varying benefits for different programs. 40% of the programs can be speeded up by a factor 2, while 30% of the programs can be speeded up by a factor 3. Which option would be better ? **(7)**

ii) Choose any four multicore architectures which you have studied, analyze their advantages and disadvantages and present a summary of it. **(8)**

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