ANNA UNIVERSITY OF TECHNOLOGY, COIMBATORE

B.E. / B.TECH. DEGREE EXAMINATIONS : NOV / DEC 2011

REGULATIONS : 2008

THIRD SEMESTER

080230012 - DIGITAL PRINCIPLES AND SYSTEM DESIGN

(COMMON TO CSE / IT)

Time : 3 Hours   Max. Marks : 100

PART - A

(10 x 2 = 20 MARKS)

ANSWER ALL QUESTIONS

1.   Convert the binary $(11011.01001)_2$ into decimal number.

2.   What are the different ways to represent a negative number?

3.   Define non weighted codes.

4.   Name the types of modeling techniques used in HDL.

5.   Differentiate between PAL and PLA.

6.   What is meant by data distributer?

7.   How many flip flops are required for designing synchronous MOD 50 counter.

8.   Distinguish mealy and Moore models.

9.   Write the use of implication table.

10. Name the different types of Hazards.

PART – B

(5 x 16 = 80 Marks)

ANSWER ALL QUESTIONS

11. a) Find the SOP form using a Karnaugh map.

$$F=\Sigma(0,1,6,7,9,13,14,15,16,17,32,33,38,39,46,47,48,49,57,61)$$ and also write the advantages over tabulation method.

(OR)

b)   State and prove the postulates and theorems of Boolean algebra, with Illustration.

12. a) i.)Show that the Excess – 3 code is self complementing.   8

ii.) Show that if a weighted code is self complementing, then the algebra   8

sum of the weights equals nine.

(OR)

b)   i) Explain in detail about BCD adder.   8

ii) Design a full adder circuit using two half adder.   8

13. a)   Combinational circuits is defined by the following functions $f1=\Sigma(1,3,5)$, $f2=\Sigma(5,6,7)$. Implement the circuit with the PLA.

(OR)

b)   Design a decoder circuit using Full adder and also write the HDL coding for two-to-four line decoder.

14. a) A sequential circuit has one flip flop with output 2, two inputs x and y and one output. It consists of a full adder circuit connected to a D-flip flop. Derive the state table and state diagram.

(OR)

b) Design a shift register with parallel load that operate according to the following function table.

Shift	Load	Register Operati
0	0	No change
0	1	Load parallel da
1	x	Shift right

15. a) Design a MOD 10 counter using JK-flip flop.

(OR)

b) How hazards are overcome by combinational circuit and sequential circuit, explain with suitable examples.

*****THE END*****

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