Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 97042

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2014.

Second Semester

Computer Science and Engineering

CS 6201 — DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Computer and Communication Engineering and Information Technology)

(Regulation 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. State the Principle of duality.

2. Implement AND gate using only NOR gates.

3. Implement the following Boolean function using 8:1 multiplexer $F(A, B, C) = \Sigma m(1, 3, 5, 6)$.

4. Define hazard.

5. Distinguish Moore and Mealy circuit.

6. With reference to a JK flip flop, what is racing?

7. How many states are there in a 3-bit ring counter? What are they?

8. What is a Priority Encoder?

9. Whether PAL is same as PLA? Explain.

10. What is a volatile memory? Give example.

PART B — (5 × 16 = 80 marks)

11. (a) Simplify the function $F(w,x,y,z) = \Sigma m(2,3,12,13,14,15)$ using tabulation method. Implement the simplified function using gates. (16)

Or

(b) (i) Simplify the Boolean function in Sum of Products (SOP) and Product of Sums (POS) $F(A,B,C,D) = \Sigma m(0,1,2,5,8,9,10)$. (10)

(ii) Plot the following Boolean function in Karnaugh map and simplify it. $F(w,x,y,z) = \Sigma m(0,1,2,4,5,6,8,9,12,13,14)$. (6)

12. (a) Design and implement a 8421 to gray code converter. Realize the converter using only NAND gates. (16)

Or

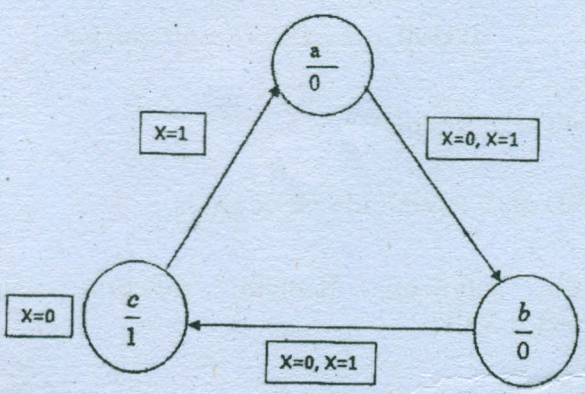
(b) Design 2-bit Magnitude Comparator and write a Verilog HDL code. (16)

13. (a) Design a MOD-10 Synchronous counter using JK flip-flops. Write execution table and state table. (16)

Or

(b) (i) How race condition can be avoided in a flip flop? (8)

(ii) Realize the sequential circuit for the state diagram shown below. (8)



14. (a) An asynchronous sequential circuit is described by the following excitation and output function. (16)

$Y = X_1X_2 + (X_1 + X_2)Y$

$Z = Y$.

(i) Draw the logic diagram of the circuit.

(ii) Derive the transition table and output map.

(iii) Describe the behaviour of the circuit.

Or

(b) Design a synchronous counter using JK flip-flop to count the following sequence 7, 4, 3, 1, 5, 0, 7.... (16)

15. (a) Design a BCD to Excess-3 code converter and implement using suitable PLA. (16)

Or

(b) Discuss on the concept of working and applications of semiconductor memories. (16)

———————