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**Question Paper Code : 51376**

**B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2016**

**Third Semester**

**Computer Science and Engineering**

**CS 2202/CS 34/EC 1206 A/080230012/10144 CS 303 – DIGITAL PRINCIPLES AND SYSTEM DESIGN**

**(Common to Information Technology)**

**(Regulations 2008/2010)**

**(Common to PTCS 2202 – Digital Principles and System Design for B.E. (Part-Time) Second Semester – CSE – Regulations 2009)**

**Time : Three Hours** **Maximum : 100 Marks**

**Answer ALL questions.**

**PART – A (10 × 2 = 20 Marks)**

1. Convert the gray code (11011) to binary code.
2. Simplify the following expression with Boolean laws :
   Y = ABC + AB'C + ABC'
3. Implement a full adder with two half adders.
4. Implement a 4-bit even parity checker.
5. Write the HDL data flow description of four bit adder.
6. Differentiate between encoder and decoder.
7. Realize a JK flip-flop using D flip-flop.
8. Write the HDL code for up-down counter using behavioural model.
9. What is primitive flow table ?
10. What are static '1' and static '0' hazards ?

## PART – B (5 × 16 = 80 Marks)

11. (a) (i) List the ASCII code for the 10 decimal digits with an odd parity in the leftmost position. **(6)**

(ii) Simplify the three variable logic expression. **(6)**

$Y = \pi M (1, 3, 5)$

(iii) Implement Y = (A'B + AB') (C + D') using NOR gates. **(4)**

**OR**

(b) Simplify the following Boolean function by using tabulation method : **(16)**

F (A,B,C,D) = Σ(1,4,6,7,8,9,10,11,15)

12. (a) (i) Analyse the combinational circuit shown in figure 12 (a) (i) to determine the truth table and the Boolean expressions governing the outputs of the circuit. **(10)**

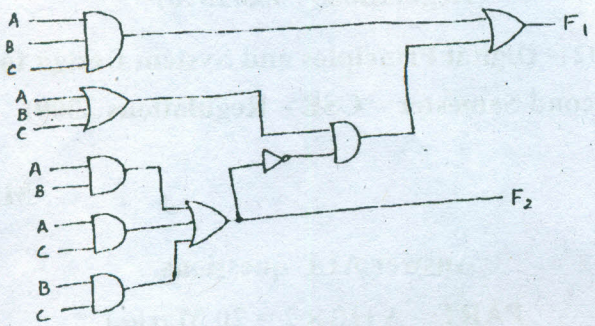


**Figure 12 (a) (i)**

(ii) Explain BCD adder with a neat block diagram. **(6)**

**OR**

(b) (i) Design a BCD to excess-3 code converter using logic gates. **(12)**

(ii) Draw the diagram of a 4-bit adder subtracter using full adders. **(4)**

13. (a) (i) Realize 4 × 16 decoder using two 3 × 8 decoders with enable input. **(4)**

(ii) Implement the two following Boolean functions using 8 × 2 PROM.

F1 = Σm (3, 5, 6, 7) and F2 = Σm (1, 2, 3, 4). **(6)**

(iii) Implement the following function using a multiplexer.

F(W, X, Y, Z) = Σm (0, 1, 3, 4, 8, 9, 15). **(6)**

**OR**

(b) Implement the following two Boolean functions using PLA with 3 inputs, 4 product terms and 2 outputs.

$F1 = \Sigma m(3, 5, 6, 7)$ and $F2 = \Sigma m(1, 2, 3, 4)$. **(16)**

14. (a) Design a sequential circuit with two T flip-flops A and B, one input X and one output Z is specified by the following next state and output equation is

$A(t + 1) = BX' + B'X$

$B(t + 1) = AB + BX + AX$

$Z = AX' + A'B'X$

(i) Draw the logic diagram of the circuit

(ii) List the state table for the sequential circuit.

(iii) Draw the corresponding state diagram. **(16)**

**OR**

(b) (i) Draw and explain the parallel in serial out shift register and explain. **(8)**

(ii) Draw the block diagram of Johnson counter and explain. **(8)**

15. (a) (i) Explain the types of hazards in digital circuits.

(ii) Implement the switching function $F = \Sigma m (1, 3, 5, 7, 8, 9, 14, 15)$ by a static hazard free 2 level AND-OR gate network.

**OR**

(b) Explain the steps for the design of asynchronous sequential circuits.

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