ANNA UNIVERSITY COIMBATORE

B.E. / B.Tech. DEGREE EXAMINATION – DECEMBER 2008

THIRD SEMESTER - CSE / IT

IT301- DIGITAL PRINCIPLES AND SYSTEM DESIGN

Time: Three Hours **Maximum: 100 Marks**

PART A – (20 x 2 = 40 Marks)

Answer ALL Questions

1. Solve $(247.36)_8 = (x)_2 = (y)_{16}$
2. Find the complement of F= x (y + z) and show that F + F' =1.
3. Realize the function Y= A + B using only NAND gate.
4. Express the minterm m_{21} using minimum number of variables.
5. Implement a full adder using two half adder & OR gate
6. Mention the need for a carry look ahead adder.
7. State the condition to check the equality of two n bit binary numbers A and B.
8. What are the applications of HDL processing?
9. Realize the following expressions using verilog HDL.

   X = A + B'C + BD

   Y = (A + B) (C' + D)
10. Draw the logic diagram of a combinational circuit which helps in data distribution.
11. Realize the function F (A, B, C) = ∑ m (1, 2, 6, 7) using a decoder.
12. What are the different types of programming the PLA?
13. Construct JK flipflop using D flipflops ?
14. Compare combinational circuit and sequential logic circuit
15. Write the HDL behavioural description of 4 bit shift registers
16. What is a race around condition?

17. Draw the hazard free circuit for the Boolean Expression

    $y = x_1x_2 + \bar{x}_2 x_3$
18. Define the fundamental mode.
19. What are the steps to be followed for the purpose of merging a flow table?
20. What is the reason for essential hazard?

PART B – (5 x 12 = 60 Marks)

Answer Any FIVE Questions

21. (a) Simplify using K-map and express the reduced expression in SOP and POS form.

    $F = \sum m (0, 6, 8, 13, 14) + \sum d (2 , 4, 10)$ (8)

    (b) Reduce the following Boolean expression

    $F = (x' y' + z)' + z + x y + w z$ (4)

22. Solve the given Boolean function using Quine MC Cluskey method and draw the logic diagram for the reduced expression using only NOR gates.

    $F(A, B, C ,D) = \sum m(1,3,5,7,9,15) + \sum d (4,6,12,13)$ (12)

23. Design a code converter that converts a decimal digit from the 8, 4, -2, -1 code to BCD. (12)

24. (a) Write down the behavioral description of a 4 to 1 line Multiplexer. (4)

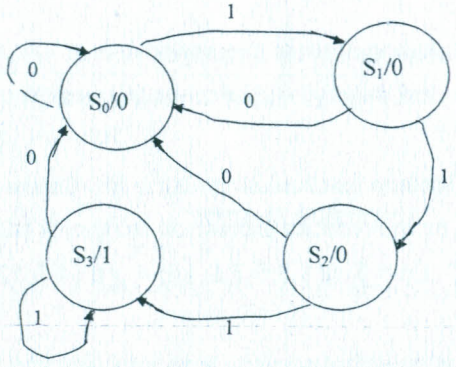
(b) Implement the following two Boolean functions using a PLA.

$$A(x, y, z) = \sum m\,(1, 2, 4, 6)$$

$$B(x, y, z) = \sum m\,(0, 1, 2, 6)$$ (8)

25. Design a parallel counter which counts the sequence 0, 1,2,5,6,7 using JK flipflops. (12)

26. Design a sequential circuit specified by the given state diagram of a sequence detector using 'D' flip flops . (12)



27. Explain the different types of hazards in combinational circuits and Sequential circuits with an example. (12)

28. (a) Obtain a primitive flow table for an asynchronous sequential circuit with 2 inputs x, y and output Q. The output Q = x as long as y =1 and retains this value after y goes to 0. Once y goes to 0, a change in x does not change the value of output Q. (8)

(b) Assign output values to don't cares in the flow table to avoid transient output pulses. (4)

	00	01	11	10
a	*a*,0	*b*,–	–,–	*d*,–
b	*a*,–	*b*,1	*b*,1	*c*,–
c	*b*,–	–,–	*b*,–	*c*,0
d	*c*,–	*d*,1	*c*,–	*d*,1

*********THE END*********