ANNA UNIVERSITY COIMBATORE

B.E. / B.TECH. DEGREE EXAMINATIONS : DECEMBER 2009

REGULATIONS : 2007

THIRD SEMESTER

070250002 - DIGITAL PRINCIPLES AND SYSTEM DESIGN

(COMMON TO CSE / IT)

TIME : 3 Hours Max.Marks : 100

PART – A

(20 x 2 = 40 MARKS)

ANSWER ALL QUESTIONS

1. Define: positive logic and negative binary logic system.
2. Write notes on minterms and maxterms?
3. State principle of duality.
4. Simplify the following Boolean functions: a)AB+A'D+BD b) (A+B)(A+B')
5. What is magnitude comparator?
6. What you meant by BCD addition its differ from Decimal addition?
7. What is carry look ahead principle in parallel adder?
8. Write gate level description of a 2 to 4 decoder.
9. Write down a design procedure of combinational logic circuit.
10. What is three state logic gates and its applications?
11. Write a truth table of 4 input priority encoder.
12. What is meant by the term 'edge triggered'.
13. What are mealy and Moore machines?
14. Distinguish between PLA and PAL.
15. Derive the characteristic equation of a JK flip-flop.
16. What are the applications of shift register?
17. What is meant by race?
18. State that fundamental mode.
19. What is a static 1 Hazard?

20. How to detect and eliminate hazards from an asynchronous network?

PART – B

(5 x 12 = 60 MARKS)

ANSWER ANY FIVE QUESTIONS

21. Find a minimum sum of products expression for the following function using Quine-McCluskey method, f(A,B,C,D,E)=Σ(0,1,2,8,9,15,17,21,24,25,27,31)

22. a Using K-map, find the MSP form of F(a,b,c,d)= Σ(0,1,2,4,5,6,8,912,13,14,) 8

b Obtain the canonical product of sum form of the function Y(a,b,c,)=ab+a'c 4

23. Design a combinational circuit which accepts 4 bit BCD number and converts its equivalent excess 3 code.

24. Write a gate level hierarchical description of 4 bit adder using verilog HDL.

25. Explain how you will build a 16 input MUX using only 4 input MUXs.

26. a Explain the operation of JK and clocked JK flip-flops with suitable diagrams. 8

b What is race around condition? How is it avoided? 4

27. Design a BCD Ripple counter using JK FF implement and explain.

28. An asynchronous sequential machine operating in fundamental mode has 2 input lines x1 and x2 and one output z. The output is zero whenever x2 is '0' with the first change in x1 occurring while x2 is 1, Z remains '1' until x2 returns to zero. Write down a state table for this machine and draw logic diagram.

*****THE END*****