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Question Paper Code : 91340

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2014.

Third Semester

Computer Science and Engineering

CS 2202/CS 34/EC 1206 A/080230012/10144 CS 303 — DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Information Technology)

(Regulation 2008/2010)

(Common to PTCS 2202 – Digital Principles and System Design for B.E. (Part-Time) Second Semester – CSE – Regulation 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert $(A3B)_H$ into decimal numbers.

2. Find the complement of the function $F = x'yz' + x'y'z$.

3. Define a code converter logic circuit.

4. What is a Half adder? Write its truth table.

5. List out the applications of Multiplexer.

6. Distinguish between de-multiplexer and decoder.

7. Write down the characteristic equation of S–R flip–flop.

8. Explain the difference between the performance of asynchronous and synchronous counters.

9. Write down the steps involved in the design of synchronous sequential circuits.

10. Define Races in asynchronous sequential circuits.

PART B — (5 × 16 = 80 marks)

11. (a) Find the minimal sum of products for the Boolean expression $F(w,x,y,z) = \Sigma(1, 3, 4, 5, 9, 10, 11) + \Sigma\phi\ (6, 8)$ using Quine McCluskey method.

Or

(b) Simply the following Boolean function using five variable map :

F(A, B, C, D, E) = A'B'CE' + B'C'D'E' +A'B'D' + B'CD'+A'CD +A'BD

12. (a) Design a Binary to Gray code converter circuit.

Or

(b) (i) Design a half subtractor with inputs x and y and outputs Diff and Bout. The circuit subtracts the bits x-y and places the difference in Diff and the borrow in B_{out}.

(ii) Design a Full subtractor with three inputs x, y, and B_{in} and two outputs Diff and B_{out}. The circuit subtracts $x - y - B_{in}$ where B_{in} is the input borrow, B_{out} is the output borrow, and diff is the difference.

13. (a) Design a BCD to seven segment decoder circuit.

Or

(b) (i) Construct a 16 × 1 multiplexer with two 8 × 1 and one 2 × 1 multiplexers. Use Block diagrams.

(ii) Write the HDL gate level description of the priority encoder circuit.

14. (a) Explain the operation of Master Slave flip–flop and show how the race around condition is eliminated in it.

Or

(b) Design a MOD 6 counter circuit.

15. (a) A asynchronous sequential circuit has two internal states and one output. The two excitation functions and one output function describing the circuit are, respectively,

$Y_1 = x_1x_2 + x_1y_2' + x_2'y_1$

$Y_2 = x_2 + x_1y_1'y_2 + x_1'y_1$

$Z = x_2 + y_1$

(i) Draw the logic diagram of the circuit.

(ii) Derive the transition table and output map.

(iii) Obtain a flow table for the circuit.

Or

(b) Design an asynchronous sequential circuit that has two inputs x_1 and x_2 and one output Z. The output $Z = 1$ if x_1 changes from 0 to 1, $Z = 0$ if x_2 changes from 0 to 1, and Z = 0 otherwise. Realise the circuit using D flip flops.