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## Question Paper Code : 80285

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2016.

Second Semester

Computer Science and Engineering
CS 6201 - DIGITAL PRINCIPLES AND SYSTEM DESIGN
(Common to Information Technology)
(Regulations 2013)
Time : Three hours
Maximum : 100 marks
Answer ALL questions.

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\text { PART A }-(10 \times 2=20 \text { marks })
$$

1. State the principle of duality.
2. State and prove the Consensus Theorem.
3. What is priority encoder?
4. Draw the circuit for 2-to-1 multiplexer.
5. What is the operation of JK flip flop?
6. Define race around condition.
7. Define flow table in asynchronous sequential circuit.
8. What are races?
9. How to detect double error and correct single error?
10. Give the comparison between EPROM and PLA.
11. (a) (i) Minimize the following expression using Karnaugh map.

$$
\begin{equation*}
Y=A^{\prime} B C^{\prime} D^{\prime}+A^{\prime} B C^{\prime} D+A B C^{\prime} D^{\prime}+A^{\prime} B^{\prime} C D^{\prime} \tag{8}
\end{equation*}
$$

(ii) State and prove the Demorgan's theorem.

Or
(b) (i) Implement the switching function $f(x, y, z)=$ $\sum m(0,1,3,4,12,14,15)$ with NAND gates.
(ii) Minimize the following expression using Quine Mccluskey method.

$$
\begin{equation*}
Y=A^{\prime} B C^{\prime} D^{\prime}+A^{\prime} B C^{\prime} D+A B C^{\prime} D^{\prime}+A B C^{\prime} D+A B^{\prime} C^{\prime} D+A^{\prime} B^{\prime} C D^{\prime} \tag{8}
\end{equation*}
$$

12. (a) (i) Compare and contrast between encoder and multiplexer.
(ii) Design a combinational circuit to convert binary to gray code.

Or
(b) (i) Design a combinational circuit that converts 8421 BCD code to excess-3 code.
(ii) With neat diagram explain the 4 bit adder with carry look ahead. (8)
13. (a) (i) Implement JK flip flop using D flip flop.
(ii) How the race condition can be avoided in a flip flop?

Or
(b) Consider the design of 4 -bit BCD counter that counts in the following way:
$0000,0001,0010 \ldots ., 1001$ and back to 0000. Draw the logic diagram of this circuit.
14. (a) Explain the steps for design of asynchronous sequential circuits.

$$
\mathrm{Or}
$$

(b) Explain the types of hazards in combinational circuits and sequential circuits and also demonstrate a hazard and its removal with example.
15. (a) Implement the following using PLA.

$$
\begin{align*}
& A(x, y, z)=\sum m(1,2,4,6) \\
& B(x, y, z)=\sum m(0,1,6,7) \\
& C(x, y, z)=\sum m(2,6) \tag{16}
\end{align*}
$$

Or
(b) Discuss on the concept of working and applications of semiconductor memories.

