ANNA UNIVERSITY COIMBATORE

B.E. / B.TECH. DEGREE EXAMINATIONS : SEPTEMBER 2009

REGULATIONS - 2007

THIRD SEMESTER

070250002 – DIGITAL PRINCIPLES AND SYSTEM DESIGN

(COMMON TO CSE / IT)

TIME : 3 Hours **Max.Marks : 100**

PART – A

(20 x 2 = 40 MARKS)

ANSWER ALL QUESTIONS

1. Convert the octal number $(623.77)_8$ to hexadecimal.
2. What does duality principle state?.
3. Simplify the Boolean function (xyz+x'y+xyz') to a minimum number of literals.
4. Write the truth table of three input Exclusive - OR
5. Simplify (A+B)(A+B) = A+B + A+B using Demorgan's theorem
6. What is the Excess-3 equivalent for the BCD number 1001.
7. Implement AND gate using only NOR.
8. Expand VHDL.
9. Differentiate encoder and decoder.
10. Mention any two applications of Multiplexer.
11. What are the different types of ROM?.
12. What is FPGA ?.
13. Differentiate combinational and sequential circuits.
14. How the MSI circuits are classified?.
15. What do you mean by a counter?.
16. What is T-flip flop?. How it is obtained?.
17. Mention the different types of design units in VHDL.
18. What is a fundamental mode asynchronous circuit?
19. When do hazards occur?

20. What is the cause behind essential hazard?

PART – B

(5 x 12 = 60 MARKS)

ANSWER ANY FIVE QUESTIONS

21. a) What is Karnaugh map?. Simplify the Boolean function using sum of products and also draw the gate implementation of the given function $F(A,B,C,D)= \sum(0,1, 2, 5, 8, 9, 10)$ 8

    b) Prove (A+B)(A+C) = A + BC 4

22. a) Simplify the Boolean function $F(w,x,y,z)= \sum(1, 3, 7, 11, 15)$ and the don't care conditions : $d(w,x,y,z)= \sum(0, 2, 5)$ using either sum of products or products of sums. 6

    b) Design a Full adder using two half adder circuits and prove it. 6

23. a) Design a logic circuit that has three inputs A,B and C whose output will be HIGH only when a majority of the inputs are HIGH. 8

    b) Advantage of using HDL for combinational logic circuits. 4

24. Define code convertor. Explain BCD to excess 3 code convertor with truth table and logic diagram.

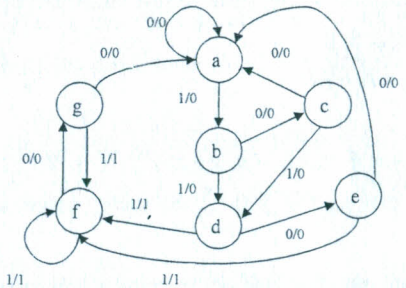
25. a) Design a 3-to-8 BCD to decimal decoder. 8

    b) Write briefly about PLA. 4

26. a) Design a 4-bit binary ripple counter. 6

    b) Explain the D-Flip flop with a diagram. 6

27. a) For the state diagram shown in fig. Derive the reduced state table and state assignment. 8



b) What is a shift register?. If a serial – in – serial – out shift register has 'n' stages and if the clock frequency is 'f' Hz, what will be the time delay between input and output?. 4

28. a) Write short notes on Static Hazards 6

b) Write short notes on Races. 6

*****THE END*****