Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 31298

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2013.

Third Semester

Computer Science and Engineering

CS 2202/CS 34/EC 1206 A/10144 CS 303/080230012 — DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Information Technology)

(Regulation 2008/2010)

(Common to PTCS 2202 – Digital Principles and System Design for B.E. (Part-Time) Second Semester – CSE – Regulation 2009)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert $(1001010.1101001)_2$ to base 16 and $(231.07)_8$ to base 10.

2. Realize XOR gate using only 4 NAND gates.

3. Implement $F = XY'Z + Y'Z' + X'Z$ using AOI logic.

4. Obtain the truth table for BCD to Excess-3 code converter.

5. Draw the truth table and circuit diagram of 4 to 2 encoder.

6. Distinguish EEPROM and flash memory.

7. Realize a JK flip-flop using D flip-flop be and gates.

8. Write the HDL code for up-down counter using behavioral model.

9. Distinguish fundamental mode circuit and pulse mode circuit.

10. Define primitive flow table.

PART B — $(5 \times 16 = 80$ marks)

11. (a) Simplify the following Boolean function using Quine-McClusky method $F = (A, B, C, D, E) = \Sigma m(0, 1, 3, 7, 13, 14, 21, 26, 28) + \Sigma d(2, 5, 9, 11, 17, 24)$. (16)

Or

(b) (i) Simplify the given Boolean function in POS form using K-map and draw the logic diagram using only NOR gates.

$$F(A, B, C, D) = \pi M\ (0, 1, 4, 7, 8, 10, 12, 15) + d(2, 6, 11, 14). \quad (10)$$

(ii) Convert 78.5_{10} into binary. (3)

(iii) Find the dual and complement of the following Boolean expression. $xyz' + x'yz + z(xy + w)$. (3)

12. (a) Design a combinational circuit to perform BCD addition. (16)

Or

(b) (i) Design a 4-bit magnitude comparator with three outputs: $A > B$, $A = B$ & $A < B$. (12)

(ii) Construct a 4-bit odd parity generator circuit using gates. (4)

13. (a) (i) Realize 4×16 decoder using two 3×8 decoders with enable input. (4)

(ii) Implement the two following Boolean functions using 8×2 PROM.

$$F1 = \Sigma m(3, 5, 6, 7) \text{ and } F2 = \Sigma m(1, 2, 3, 4). \quad (6)$$

(iii) Implement the following function using a multiplexer.

$$F(W, X, Y, Z) = \Sigma m(0, 1, 3, 4, 8, 9, 15). \quad (6)$$

Or

(b) Implement the following two Boolean functions using PLA with 3 inputs, 4 product terms and 2 outputs.

$$F1 = \Sigma m(3, 5, 6, 7) \text{ and } F2 = \Sigma m(1, 2, 3, 4). \quad (16)$$

14. (a) Design a synchronous counter with the following sequence: 0,1,3,7,6,4 and repeats. Use JK flip-flops. (16)

Or

(b) Design the sequential circuit specified by the following state diagram Q.No. 14(b) using T flip-flops. (16)

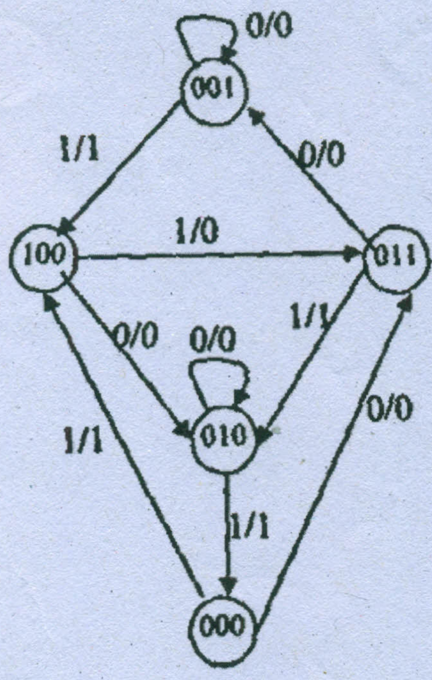

Fig. Q. 14(b)

15. (a) (i) What is the objective of state assignment in asynchronous circuit? Explain race-free state assignment with an example (8)

(ii) Discuss about static, dynamic and essential hazards in asynchronous sequential circuits. (8)

Or

(b) Design an asynchronous sequential circuit with inputs x1 and x2 and one output z. Initially and at any time if both the inputs are 0, output is equal to 0. When x1 or x2 becomes 1, z becomes 1. When second input also becomes 1, z = 0; The output stays at 0 until circuit goes back to initial state. (16)