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Question Paper Code : 10260

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2012.

Third Semester

Computer Science and Engineering

CS 2202/141302/CS 34/EC 1206 A/10144 CS 303/080230012 —
DIGITAL PRINCIPLES AND SYSTEMS DESIGN

(Common to Information Technology)

(Regulation 2008)

Time : Three hours   Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Write the application of gray code.

2. The solution to the quadratic equation $x^2 - 11x + 22 = 0$ is $x = 3$ and $x = 6$. What is the base of the numbers?

3. Define Tri-state gates.

4. Define Logic Synthesis and Simulation.

5. Write an HDL behavioral description of a 4-bit comparator with a 6-bit output y[5;0]. Bit 5 of y is for equal, bit 4 for unequal, bit 3 for greater than, bit 2 for less than, bit 1 for greater than or equal, and bit 0 for less than or equal to.

6. Write the stimulus for 2-to-1 line multiplexer.

7. Write the characteristic table and equation of JK flip flop.

8. Write any two applications of shift register.

9. Define Race Condition.

10. What is meant by essential hazards?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Define Prime Implicant and Essential Prime Implicant. (4)

    (ii) Write the procedure for obtaining the logic diagram with NAND gates from a Boolean function. (4)

    (iii) Implement the switching function. (8)

    $F(x,y,z) = \Sigma m\,(1, 2, 3, 4, 5, 7)$ with NAND gates.

Or

    (b) Minimize the expression using Quine McCluskey (Tabulation) method

    $Y' = A'BC'D' + A'BC'D + ABC'D' + ABC'D + AB'C'D + A'B'CD'$

12. (a) Design Half and Full Substractor circuits.

Or

    (b) Design a circuit that converts 8421 BCD code to Excess-3 code.

13. (a) Implement the following function using PLA

    $A(x,y,z) = \Sigma m\,(1, 2, 4, 6)$
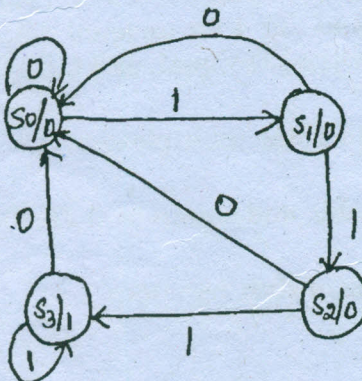
    $B(x,y,z) = \Sigma m\,(0, 1, 6, 7)$

    $C(x,y,z) = \Sigma m\,(2, 6)$

Or

    (b) Implement a full adder with two 4 × 1 multiplexers.

14. (a) (i) Draw a 4-bit ripple counter with D flip flops. (6)

    (ii) Write the HDL for the above circuit. (10)

Or

    (b) Design the sequential circuit specified by the state diagram using JK flip flop.

15. (a) Design an asynchronous sequential circuit that has 2 inputs X2 and X1 and one output Z. When X1 = 0, the output Z is 0. The first change in X2 that occurs while X1 is 1 will cause output Z to be 1. The output Z will remain 1 until X1 returns to 0.

Or

(b) Find a circuit that has no static hazards and implements the Boolean function $F(A, B, C, D) = \Sigma m \, (1, 3, 5, 7, 8, 9, 14, 15)$

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