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Question Paper Code : 91397

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2014.

Third Semester

Electronics and Communication Engineering

EC 2203/EC 34/080290010/10144 EC 304 — DIGITAL ELECTRONICS

(Regulation 2008/2010)

(Common to PTEC 2203 – Digital Electronics for B.E. (Part – Time) Third Semester – Electronics and Communication Engineering Regulation 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Simplify : $A\overline{B}C+\overline{A}\,\overline{B}C$.

2. Write the truth table for EXOR gate.

3. State the function of select inputs of a MUX.

4. Draw the logic circuit of a half subtractor.

5. Mention the advantage of JK - FF over SR - FF.

6. Draw the basic block diagram of sequential circuits.

7. How many address lines are required for a 4K ROM?

8. List the types of PLDs.

9. Compare Mealy and Moore machines.

10. Differentiate between static and dynamic hazards.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Simplify the Boolean function $F = \pi(1,3,5,6,7,10,14,15)$ and realize using NAND gates only. (10)

(ii) Briefly about the CMOS characteristics. (6)

Or

(b) (i) Using tabulation method minimize the following function $F = \sum(0,1,2,8,9,15,17,21,24,25,27,31)$. (10)

(ii) Simplify the expression $Y = AB + A\overline{B}.\overline{(\overline{A}\,\overline{C})}$. (6)

12. (a) (i) Implement the full subtractor using demultiplexer. (6)

(ii) Draw the circuit of a BCD adder and explain its operation. (10)

Or

(b) Design a BCD to seven segment decoder. (16)

13. (a) (i) Explain the different methods of triggering FFs. (6)

(ii) Design a synchronous MOD 12 down counter using JK FFs. (10)

Or

(b) (i) Explain how to convert serial data to parallel and parallel data to serial using shift registers. (10)

(ii) Realize D and T FFs using JK FF. (6)

14. (a) (i) Derive the PLA programming table for the combinational circuit that squares a 3 bit number. Minimize the number of product terms. (10)

(ii) Differentiate between

(1) Static and dynamic memory.

(2) Primary and secondary memory. (6)

Or

(b) (i) Describe the memory read and memory write operation with timing waveforms. (8)

(ii) What is FPGA? Explain. (8)

15. (a) (i) What is the significance of state assignment? Explain the different techniques used for state assignment. (8)

(ii) Design a sequence detector to detect the sequence 101 from 10101. (8)

Or

(b) (i) Give an account for various hazards that could occur in a asynchronous circuit. With examples explain how they could get eliminated. (8)

(ii) Write the HDL code for a 4 bit comparator and universal shift register. (8)
