Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 97059

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2014

Third Semester

Electronics and Communication Engineering

EC 6302 — DIGITAL ELECTRONICS

(Common to Mechatronics Engineering and Robotics and Automation Engineering)

(Regulation 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Simplify the following Boolean expression into one literal

   $W'X(Z' + YZ) + X(W + Y'Z)$.

2. Draw the CMOS inverter circuit.

3. Construct 4-bit parallel adder/subtractor using Full adders and XOR gates.

4. Convert a two-to-four line decoder with enable input to 1×4 demultiplexer.

5. Realize JK flip flops.

6. How does ripple counter differ from synchronous counter?

7. Compare and contrast EEPROM and flash memory.

8. What is a Field Programmable Gate Arrays (FPGA) device?

9. Define ASM chart. List its three basic elements.

10. What is critical race condition in asynchronous sequential circuits? Give an example.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Convert the following function into Product of Max-terms.

$F(A,B,C) = (A + B')(B + C)(A + C')$. (4)

(ii) Using Quine McClusky method, simplify the given function.

$F(A,B,C,D) = \Sigma m(0, 2, 3, 5, 7, 9, 11, 13, 14)$. (12)

Or

(b) (i) Draw the multiple-level two input NAND circuit for the following expression : $F = (AB' + CD')E + BC(A + B)$. (4)

(ii) Draw and explain Tri-state TTL inverter circuit diagram and explain its operation. (12)

12. (a) (i) Design a 4-bit decimal adder using 4-bit binary adders. (10)

(ii) Implement the following Boolean functions using Multiplexers

$F(A,B,C,D) = \Sigma m(0, 1, 3, 4, 8, 9, 15)$. (6)

Or

(b) (i) Design a 4-bit magnitude comparator with three outputs : A > B, A = B and A < B. (12)

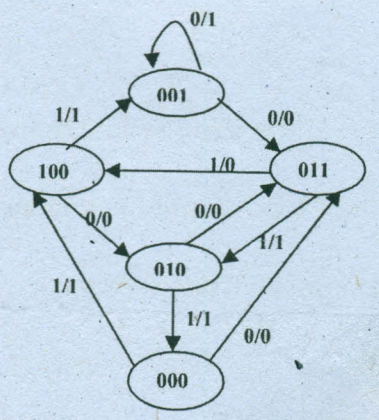
(ii) Construct a 4-bit even parity generator circuit using gates. (4)

13. (a) (i) Design a 3-bit synchronous counter using JK flip-flops. (12)

(ii) Explain the differences between a state table, a characteristic table and an excitation table. (4)

Or

(b) Design the sequential circuit specified by the following state diagram using T flip-flops. Check whether your design is self-correctable. (16)



14. (a) (i) Write short notes on EAPROM and static RAM cell using MOSFET. (6)

(ii) Using eight 64 × 8 ROM chips with an enable input and a decoder, construct a 512 × 8 ROM. (10)

Or

(b) (i) Use PLA with 3 inputs, 4 AND terms and two outputs to implement the following two Boolean functions. (12)

$F1(A, B, C) = \Sigma m(3,5,6,7)$ and $F2(A, B, C) = \Sigma m(1, 2, 3, 4)$

(ii) Compare and contrast PLA and PAL. (4)

15. (a) (i) What is a hazard in an asynchronous sequential circuits? Define static hazard, dynamic hazard and essential hazard. (6)

(ii) Write and verify the HDL structural description of the four-bit register with parallel load. Use a 2 × 1 multiplexer for the flip-flop inputs. Include an asynchronous clear input. (10)

Or

(b) Design an asynchronous sequential circuit with inputs A and B and an output Y. Initially and at any time if both the inputs are 0, the output, Y is equal to 0. When A or B becomes 1, Y becomes 1. When the other input also becomes 1, Y becomes 0. The output stays at 0 until circuit goes back to initial state. (16)