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Question Paper Code : 21444

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2015.

Third Semester

Electronics and Communication Engineering

EC 2203/EC 34/080290010/10144 EC 304 – DIGITAL ELECTRONICS

(Regulations 2008/2010)

(Common to PTEC 2203 – Digital Electronics for B.E. (Part-Time) Third Semester – Electronics and Communication Engineering Regulations 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Simplify the given Boolean expression using De Morgan's theorem $F = \overline{A\left(\overline{B+\overline{C}}\right)D}$.

2. Design a 3 input CMOS NAND gate.

3. Draw a Half adder using NAND gates.

4. Draw the logic diagram of 4:1 multiplexer.

5. What is the advantage of using master–slave JK flipflops?

6. Design a 3-bit ring counter.

7. Draw the logic diagram of bipolar RAM cell.

8. Differentiate static and dynamic RAM.

9. List the types of hazards that exist in asynchronous sequential circuits.

10. Model a D-Flipflop using verilog.

PART B — (5 × 16 = 80 marks)

11. (a) Simplify the given Boolean function using Quine McCluskey method $F = \sum m(0,1,2,4,5,6,8,9,12,13,14)$. Realise the simplified function using logic gates. (16)

Or

(b) (i) Determine the Boolean expression for the logic circuit shown in Fig. 11(b)(i). Simplify the Boolean expression. (8)

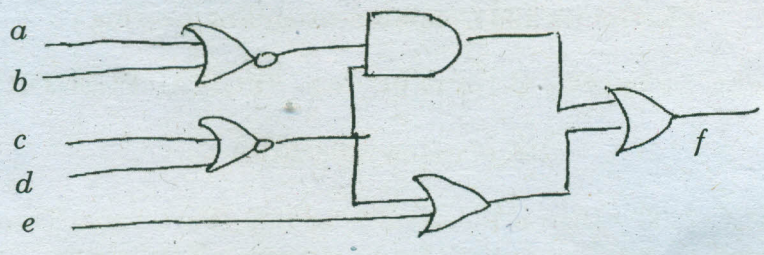

Fig. 11 (b) (i)

(ii) Using K-map method, simplify the given Boolean function and obtain minimum POS expression.

$X = \sum m(0,2,3,6,7) + \sum d(8,10,11,15)$. (8)

12. (a) Design a BCD adder and explain its operation. (16)

Or

(b) Design a BCD to excess 3 code converter. (16)

13. (a) (i) Design a 4 bit asynchronous up/down counter using JK flipflops. (8)

(ii) Design a mod-10 synchronous counter using D-flipflops. (8)

Or

(b) (i) Draw the logic diagram of a 4-bit universal shift register and explain its operation. (10)

(ii) Design a 4 bit serial adder. (6)

14. (a) Explain in detail about memory decoding and memory expansion. (16)

Or

(b) How the programmable logic devices are classified? Explain each one of them in detail.

15. (a) Analyse the given synchronous sequential circuit shown in Fig. 15(a). (16)

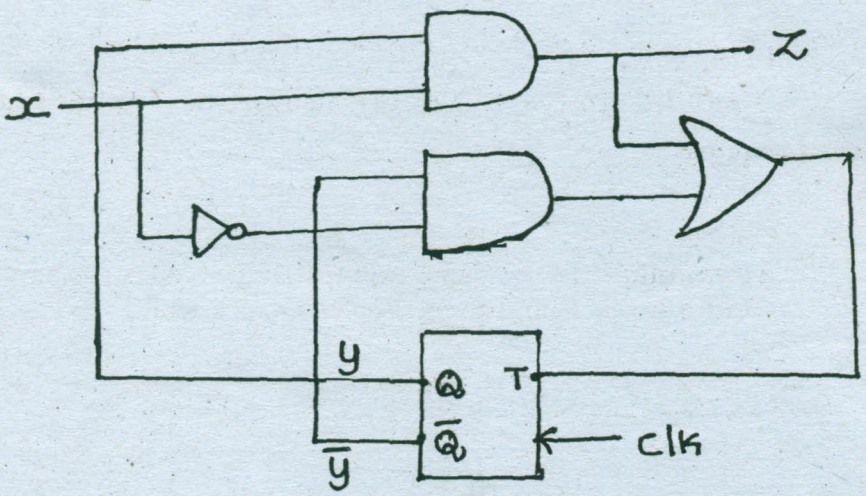

Fig. 15(a)

Or

(b) Using verilog model the given circuits.

(i) 3:8 Decoder. (8)

(ii) 2 bit up/down synchronous counter. (8)