

ANNA UNIVERSITY COIMBATORE

B.E. / B.TECH. DEGREE EXAMINATIONS : DECEMBER 2009

REGULATIONS - 2007

FOURTH SEMESTER – ELECTRICAL AND ELECTRONICS ENGINEERING

070290005 - DIGITAL ELECTRONICS

TIME : 3 Hours

Max.Marks : 100

PART – A

(20 x 2 = 40 MARKS)

ANSWER ALL QUESTIONS

1. Find the excess-3 code and its 2's complement for the decimal number 596.
2. What bit must be complemented to change an ASCII letter from uppercase to lowercase and lower case to upper case?
3. Simplify the following Boolean expression to a minimum number of literals:  
 $(X+Y)(X+\bar{Y})$
4. State the rules in Boolean algebra.
5. Why digital circuits are more frequently constructed with NAND or NOR gates than with AND and OR gates?
6. Design an EX-OR gate using only NAND gate.
7. Differentiate between decoder and demultiplexer.
8. Draw the circuit of a half adder-subtractor
9. What is race around condition? How is it avoided?
10. Distinguish between a combinational logic circuit and sequential logic circuit.
11. Draw the complete timing diagram for the five-stage synchronous binary counter.
12. If the input frequency of a T-Flipflop is 1200kHz, what will be the output frequency? Justify your answer.

13. What are the steps for the analysis and design of asynchronous sequential circuits?
14. Define a fundamental mode asynchronous sequential circuit.
15. Compare and contrast the logic families: TTL and CMOS.
16. An asynchronous sequential circuit is described by the given excitation and output function:  $Y=X_1X_2+(X_1+X_2)Y$  and  $Z=Y$ . Draw the logic diagram of the circuit.
17. What are the various classifications of semiconductor memories?
18. Define a 'memory location', 'a cell' and 'volatile memory'.
19. List the various advantages and commercially available programmable Logic Arrays (PLAs).
20. "PALs can have flip flops at the output" – Justify the statement.

PART – B

(5 x 12 = 60 MARKS)

ANSWER ANY FIVE QUESTIONS

21. a) Write notes on error detecting and correcting codes (6)  
b) Reduce the following function using Karnaugh map technique (6)  
 $F(W,X,Y,Z)=\sum m(0,7,8,9,10,12)+\sum d(2,5,13)$
22. a) Simplify the following Boolean function by using Quine Mccluskey method. (8)  
 $F(A,B,C,D)=\sum m(0,2,3,6,7,8,10,12,13)$   
b) State and Prove Demorgan's theorem (4)

23. a) Draw and explain the circuit for 3-to-8 decoder and explain. (7)
- b) Implement the following Boolean function using 4:1 MUX. (5)
24. a) Design a Full Adder circuit and Gray code converter. (8)
- b) Design a full subtractor circuit using demultiplexer. (4)
25. a) Draw and explain the working of RS-Flipflop and clocked JK – Flipflop. (8)
- b) Draw the state diagram and characteristic equation of T-Flipflop. (4)
26. a) Draw and explain the working of 4-bit up/ $\overline{down}$  synchronous counter. (6)
- b) Design a divide-by-5 ripple counter using JK-Flipflops. (6)
27. a) Design an asynchronous sequential circuit that has two inputs  $X_2$  and  $X_1$  and one output Z. When  $X_1=0$ , the output Z is 0. The first change in  $X_2$  that occurs while  $X_1$  is 1 will cause output Z to be 1. The output Z will remain 1 until  $X_1$  returns to 0. (8)
- b) Write notes on ECL logic families (4)
28. a) Discuss on the concept of working and applications of following memories: (6)
- i) ROM ii) EPROM
- b) Describe the concept, working and applications of programmable array logic and FPGA. (6)