ANNA UNIVERSITY COIMBATORE

B.E. / B.TECH. DEGREE EXAMINATIONS : JUNE 2009

REGULATIONS : 2007

FOURTH SEMESTER : ELECTRICAL & ELECTRONICS ENGG.

070290005 - DIGITAL ELECTRONICS

TIME : 3 Hours **Max.Marks : 100**

PART – A

(20 x 2 = 40 MARKS)

ANSWER ALL QUESTIONS

1. State DeMorgan's theorem.
2. Briefly explain the streamlined method of converting binary to decimal number with an example
3. Give the Gray code for the binary number $(1111)_2$
4. Subract the following: 0101 1011 – 0000 0101
5. Draw a 1 to 16 demultiplexer circuit.
6. What is priority encoder?
7. Show the common-cathode type of seven segment indicator.
8. Design a half adder using NAND gates only.
9. Draw the truth table for a NOR-gate RS filp flop
10. Obtain D Flip flop from JK flip flop.
11. Differentiate synchronous counter and Asynchronous counter.
12. Draw a modulo 6 counter.
13. What is saturation delay time? Explain
14. Compare bipolar family transistors with MOS family transistors.
15. What is a race condition? How can it be eliminated ?
16. What is essential hazard? Give an example.
17. Compare volatile data storage with non volatile data storage.

18. How is combinational logic generated in FPGA.
19. What is a DRAM? How is it refreshed ?
20. Draw a macrocell of PLD.

PART – B

(5 x 12 = 60 MARKS)

ANSWER ANY FIVE QUESTIONS

21. Simplify the following Boolean expression using three variable maps:

    a) xy+x'y'z'+x'yz'

    b) x'y'+yz+x'yz'

    c) A'B+BC'+B'C'

22. Design a 3-bit parity generator circuit and the circuit of a 4-bit parity checker using even and odd parity bit.

23. Discuss in detail about state reduction problem and state assignment problem.

24. Explain the operation of clocked masterslave J-K flipflop and D flipflop with neat diagrams.

25. Discuss in brief about the design procedure of an asynchronous circuits starting from the statement of the problem and culminates in a logic diagram.

26. Explain with a suitable example the procedure for analyzing a synchronous sequential circuit with SR latches

27. Write short notes on
    i) PAL
    ii) FPGA

28. Discuss in detail about the types of Read only memories

*****THE END*****