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Question Paper Code : 51395

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2014.

Third Semester

Electronics and Communication Engineering

EC 2203/EC 34/080290010/10144 EC 304 — DIGITAL ELECTRONICS

(Regulation 2008/2010)

(Common to PTEC 2203 – Digital Electronics for B.E. (Part-Time) Third Semester – Electronics and Communication Engineering Regulation 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Apply De-Morgan's theorem to $[(A + B) + C]'$.

2. Convert 0.35 to equivalent hexadecimal number.

3. Draw the logic circuit of a 2 bit comparator.

4. What is priority encoder?

5. Compare the logics of synchronous counter and ripple counter.

6. Sketch the logic diagram of a clocked SR flip flop.

7. Draw the structure of a static RAM cell.

8. List the advantages of PLDs.

9. What is a state diagram? Give an example.

10. Write the VHDL code for a half adder.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Given $Y(A,B,C,D) = \prod M(0,1,3,5,6,7,10,14,15)$, draw the K map and obtain the simplified expression. Realize the minimum expression using basic gates. (8)

(ii) Implement the expression $Y(A,B,C) = \prod M\ (0,2,4,5,6)$ using only NOR- NOR logic. (4)

(iii) Implement EXOR gate using only NAND gates. (4)

Or

(b) Simplify the following function using Tabulation method $Y(A,B,C,D) = \sum m(0,1,2,5,6,7,8,9,10,14)$ and implement using only NAND gates. (16)

12. (a) (i) Design a 3 : 8 decoder using basic gates. (8)

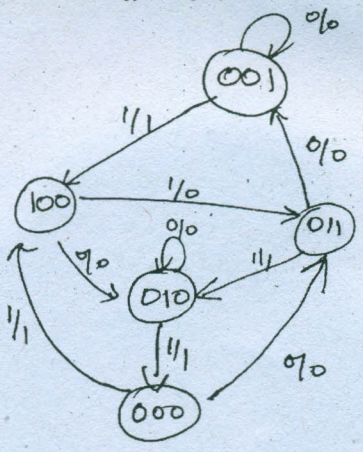
(ii) Design a binary to gray code convertor. (8)

Or

(b) (i) Design a full subtractor using demultiplexer. (8)

(ii) Explain the working of carry-look ahead adder. (8)

13. (a) Design a sequential circuit that has 3 flip-flops A, B and C, one input x and one output y .The circuit is to be designed by treating the unused states as don't care conditions. Use JK flip-flops in the design. State diagram of the circuit is as given below. (16)



Or

(b) Design a Moore type sequence detector to detect a serial input sequence of 101. (16)

14. (a) (i) Explain the read cycle and write cycle timing parameters of a RAM with the help of timing diagram. (8)

(ii) Draw the Dynamic RAM cell and explain its operation. (8)

Or

(b) Design a BCD to Excess 3 code convertor using a PLA. (16)

15. (a) Design a T flip-flop using logic gates. Derive the state table, state diagram, primitive flow table and transition table and Merger graph. Draw the logic circuit. (16)

Or

(b) Design a asynchronous sequential circuit that has 2 input's x_1 and x_2 and one output z. When $x_1 = 0$, output is 0. The change in x_2 that occurs while x_1 is 1 will cause output $z = 1$. The output z will remain 1 until x_1 returns to 0. (16)
