Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 80333

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2016.

Third Semester

Electronics and Communication Engineering

EC 6302 — DIGITAL ELECTRONICS

(Common to Mechatronics Engineering and Robotics and Automation Engineering)

(Regulations 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Simplify the following expression $X \cdot Y + X(Y + Z) + Y(Y + Z)$.

2. Why totem pole outputs cannot be connected together.

3. Write about the design procedure for combinational circuits.

4. Draw the logic diagram and truth table of Full adder.

5. Define race around condition in flip flop.

6. Draw D-latch with truth table.

7. Briefly explain about EEPROM.

8. What is programmable logic array? How it differs from ROM?

9. Define Critical race and Non Critical race.

10. What is hazard and give it types?

PART B — (5 × 13 = 65 marks)

11. (a) (i) Find the MSOP representation for $F(A, B, C, D, E) = m(1, 4, 6, 10, 20, 22, 24, 26) + d(0, 11, 16, 27)$ using K-Map method. Draw the circuit of the minimal expression using only NAND gates. (7)

(ii) With neat circuit diagram, explain the function of 3-input TTL NAND gate. (6)

Or

(b) What are the advantages of using tabulation method? Determine the Minimal sum of products for the Boolean expression $F = \sum(1, 2, 3, 7, 8, 9, 10, 11, 14, 15)$ using tabulation method. (13)

12. (a) (i) Design and explain 1 of 8 demultiplexer. (8)

(ii) What is parity checker? (5)

Or

(b) Describe the operation of 3-bit magnitude comparator. (13)

13. (a) (i) Explain the operation of JK flip-flop with neat diagram. (6)

(ii) Explain the operation of Serial- in-Serial-out shift register. (7)

Or

(b) Design synchronous MOD-6 counter. (13)

14. (a) Differentiate static and dynamic RAM. Draw the circuits of one cell of each and explain its working principle. (13)

Or

(b) Write short notes on :

(i) PAL

(ii) FPGA. (13)

15. (a) Explain the steps involved in the design of asynchronous sequential circuit.

Or

(b) Design an asynchronous circuit that will output only the second pulse received and ignore any other pulse. (13)

PART C — (1 × 15 = 15 marks)

16. (a) Design a synchronous up/down counter. (15)

Or

(b) Design an even parity generator that generates an even parity bit for every input string of 3-bits. (15)

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