Reg. No. : ☐☐☐☐☐☐☐☐☐☐☐☐

Question Paper Code : 80439

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2021.

Third Semester

Electronics and Communication Engineering

EC 2203/EC 34/080290010/10144 EC 304 – DIGITAL ELECTRONICS

(Regulations 2008/2010)

(Common to PTEC 2203 — Digital Electronics for BE. (Part—Time)
Third Semester– Electronics and Communication Engineering–Regulations 2009)

Time : Three hours   Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1.   State Distributive Law.

2.   What is Prime Implicant?

3.   Draw full adder circuit using only NAND gates.

4.   Distinguish between decoder and demultiplexer.

5.   What is the advantage of using master–slave JK flipflops?

6.   Design a 3-bit ring counter.

7.   Define Memory cycle time and Memory address setup time.

8.   Implement Half Adder using PLA.

9.   Compare mealy and moore machine.

10.   List the effects due to hazards in logic circuits.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Simplify $xy + x'z + yz$. (6)

    (ii) Simplify the following expression using K-map method.

    $Y = \Sigma m(7,9,10,11,12,13,14,15)$. (10)

    Or

    (b) (i) Write short notes on don't care conditions. (6)

    (ii) Explain about NAND and NOR implementations. (10)

12. (a) (i) Design a combinational circuit with three inputs and one output with following criteria. (8)

    (1) The output is 1 when the binary value of the inputs is less than or equal to 3. The output is 0 otherwise.

    (2) The output is 1 when the binary value of the inputs is an odd number.

    (3) The output is 1 when the binary value of the inputs is an even number.

    (ii) Implement a full adder with a decoder and NAND gates. The adder inputs are A, B and C. The adder produces outputs S and C_0 (8)

    Or

    (b) (i) Design an excess-3-code to BCD using the unused combinations of the code as don't-care conditions. (10)

    (ii) Implement the following function with a multiplexer. (6)

    $F(A,B,C,D) = \Sigma(0,2,5,7,11,14)$

13. (a) (i) Explain the operation of the Master slave JK Flip-Flop. (6)

    (ii) Design a 3-bit binary synchronous counter using T flip-flop. (10)

    Or

    (b) (i) Draw and explain the operation of a 4 bit Ripple counter with timing diagram. (8)

    (ii) Draw and explain the 4 bit Johnson shift counter. (8)

14. (a) Explain in detail about memory decoding and memory expansion. (16)

Or

(b) How the programmable logic devices are classified? Explain each one of them in detail.

15. (a) (i) Write the verilog HDL code for 'JK'FF and "T"FF. (6)

(ii) An asynchronous circuit with output changing on each rising edge of its input clock. Draw the hazard free circuit. (10)

Or

(b) (i) Draw the general model of a sequential circuit and explain. (6)

(ii) List out the steps involved in the design of synchronous sequential circuit. (10)

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