



Reg. No. :

--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--

OK/11
FN

Question Paper Code : 50434

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2017
Third Semester

Electronics and Communication Engineering
EC 6302 : DIGITAL ELECTRONICS

(Common to Mechatronics Engineering, Robotics and Automation Engineering)
(Regulations 2013)

Time : Three Hours

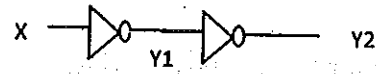
Maximum : 100 Marks

Answer ALL questions

PART – A

(10×2=20 Marks)

1. State the De Morgan's law and write any one application.
2. Sketch the waveform of each inverter output in the given diagram.



3. Draw the full adder circuit using half adder.
4. Write the function of magnitude comparator.
5. Draw the NOR gate Latch and write its truth table.
6. Write the differences between synchronous and asynchronous counters.
7. What is the memory capacity of random access memory if it has 10 bit address lines?
8. Write the types of programmable logic devices.
9. Write the difference between Moore's and Mealy model.
10. Define Hazards and list its type.

PART – B

(5×13=65 Marks)

11. a) i) Simplify the Boolean expression using laws and rules of Boolean algebra
 $Z = [AB'(C + BD) + (AB)'] \cdot C$ (7)
- ii) Define SOP and POS term. Convert the Boolean expression
 $AB'C + B'CD + AC'D$ to SOP form. (6)
- (OR)
- b) i) Implement the Boolean expression using minimum number of 3 input NAND gate
 $f(A, B, C, D) = \Sigma(1, 2, 3, 4, 7, 9, 10, 12)$. (8)
- ii) Explain the TTL circuit with open collector output. (5)



12. a) Design a 4 bit BCD adder using full adder and explain its structure and compute the circuit to add 1001 and 0101. Write the sum and carry output of the given binary number. (13)

(OR)

- b) i) Explain the operation and need of priority encoder. (7)
ii) Design a 5×32 decoder using 3×8 decoder and summarize how many decoders required designing? (6)

13. a) Draw RS flipflop circuit and explain its operation with truth table and suggest how to eliminate the undetermined stage? Write some RS Flipflop applications. (13)

(OR)

- b) Design a 4 bit binary counter and explain its counting process. Discuss how to use this circuit to perform both up and down counting. (13)

14. a) Describe the classification of semiconductor memories. (13)

(OR)

- b) Discuss the features and functional blocks of FPGA. (13)

15. a) Illustrate the design procedure of algorithmic state machine with neat flow chart. (13)

(OR)

- b) Discuss the design steps of asynchronous sequential circuits. (13)

PART – C

(1×15=15 Marks)

16. a) Design a serial 2's complement circuit with a shift register and a flipflop. The binary number is shifted out from one side and its 2's complement shifted into other side of the shift register. (15)

(OR)

- b) Select a 4096×8 bit ROM memory to store the driver program of the Robotic design. The memory chip of has two chip select inputs and operates from a 5v power supply. How many pins are needed for the integrated circuit package? Draw a block diagram and label all input and output terminals in the ROM. (15)