Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 20408

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2018.

Third Semester

Electronics and Communication Engineering

EC 6302 — DIGITAL ELECTRONICS

(Common to Mechatronics Engineering, Robotics and Automation Engineering)

(Regulations 2013)

(Also common to PTEC 6302 — Digital Electronics for B.E. (Part-time) Second Semester – Electronics and Communication Engineering – Regulations 2014)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What are the universal gates? Justify.

2. State De-Morgan's Theorem.

3. Write the characteristic equation of 4 × 1 Multiplexer.

4. State the differences between combinational and sequential circuits.

5. Draw the excitation table for D Flip Flop.

6. Draw the state diagram of 3 bit up counter.

7. Compare PAL, PLA and PROM.

8. Define setup time with timing diagram.

9. Mention the types of sequential circuits and give the difference between them.

10. Define Mealy machine with a state diagram.

PART B — (5 × 13 = 65 marks)

11. (a) Simplify f(W, X, Y, Z) = $\sum m(2, 6, 8, 9, 10, 11, 14, 15)$ using Quine – Mc Cluskey method of minimization.

Or

(b) Draw and Explain NAND, NOT and NOR gate CMOS representation.

12. (a) Draw 4 × 1 multiplexer and 1 × 4 Demultiplexer using gates and explain its operation.

Or

(b) Design a 2 bit magnitude comparator and draw its logic circuit.

13. (a) Explain the logic circuit, characteristic and excitation table of JK, SR and D flip flop.

Or

(b) Design a 3 bit synchronous binary up-down binary using T flip flop.

14. (a) Design and implement a BCD to gray code converter using PAL.

Or

(b) Write short notes on Static, Bipolar and MOSFET RAM cell.

15. (a) Elucidate the design procedure of synchronous sequential circuits.

Or

(b) Design a sequential circuit whose state tables are specified in the Table below using D flip-flops.

Present State	Next State		Output	
Q_0 Q_1	$x = 0$	$x = 1$	$x = 0$	$x = 1$
0 0	0 0	0 1	0	0
0 1	0 0	1 0	0	0
1 0	1 1	1 0	0	0
1 1	0 0	0 1	0	1

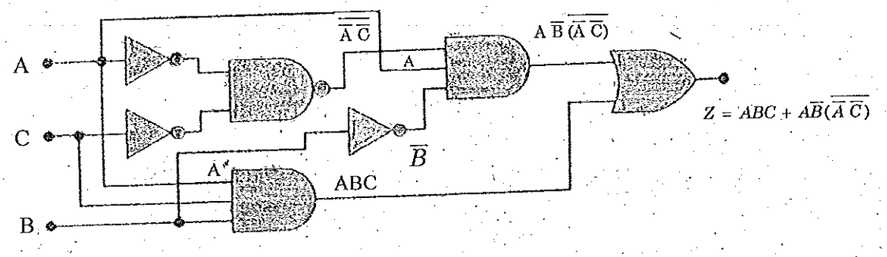
PART C — (1 × 15 = 15 marks)

16. (a) (i) Design a circuit that has a 3-bit binary input and a single output (Z) specified as follows : (8)

Z = 0, when the input is less than 5_{10}

Z = 1, otherwise

(ii) Simplify the given logic circuit using Boolean Simplification. (7)



Or

(b) Design a synchronous sequential circuit whose state diagram is shown below. (15)