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Question Paper Code : 91442

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2019

Third Semester

Electronics and Communication Engineering

EC6302 – DIGITAL ELECTRONICS

(Common to Electronics and Communication Engineering/Mechatronics Engineering/Robotics and Automation Engineering)

(Regulations 2013)

(Also Common to PTEC6302 – Digital Electronics for B.E. (Part-Time) Second Semester – Electronics and Communication Engineering – Regulations 2014)

Time : Three Hours

Maximum : 100 Marks

Answer ALL questions

PART – A

(10×2=20 Marks)

1. Simplify the given expression $Y = \overline{\left[\left(\overline{AB}\right).\overline{\overline{C}}\right]}$ using De Morgan's Theorem.
2. What is meant by a tristate gate and mention it's application ?
3. Differentiate between a conventional encoder and a priority encoder.
4. Write the function table and draw the logic diagram of a 4:1 data selector.
5. The content of a 4-bit register is initially 1101. The register is shifted 6 times to the right with the serial input being 101101. What is the content of the register after each shift ?
6. How many Flip Flops are required to build a binary counter that counts from 0 to 1023 ?
7. Differentiate between static RAM and dynamic RAM.
8. Define the terms "access time" and "cycle time" of a memory.
9. Draw the basic building blocks of an Algorithmic State Machine chart.
10. Write a Verilog behavioural model of a Transparent flip flop with reset input.

PART – B (5×13=65 Marks)

11. a) With a neat diagram, explain briefly the operation of a tristate TTL inverter circuit. Also mention how it is different from that of TTL totempole output configuration. (13)

(OR)

b) Determine a minimal SOP representation for

$f(A, B, C, D, E) = \sum m(1, 4, 6, 10, 20, 22, 24, 26) + d(0, 11, 16, 27)$ using K-map method. Draw the circuit of the minimal expression using only NAND gates. (13)

12. a) With a neat diagram, explain in detail about the concept and working principle of a carry look ahead adder circuit. (13)

(OR)

b) Design a combinational circuit that converts binary number of 4 bits to a decimal number in BCD. Note that the BCD number is same as the binary number as long as the input is less than or equal to 9. The binary number from 1010 to 1111 converts into BCD numbers from 1 0000 to 1 0101. (13)

13. a) Design a 3-bit synchronous Modulo-4 up-down counter using D Flip-flop. (13)

(OR)

b) Design a 4-bit binary ripple counter with D-Flip-flops. (13)

14. a) i) Bring out the difference between ROM, PAL and PLA. (5)

ii) Realize the following function using PAL

$F_1(x, y, z) = \sum m(1, 2, 4, 5, 7)$

$F_2(x, y, z) = \sum m(0, 1, 3, 5, 7)$. (8)

(OR)

b) i) A computer uses RAM chips of 1024×1 capacity. How many chips are needed and how should their address lines be connected to provide a memory capacity of 1024 bytes ? (5)

ii) With neat diagram, explain the operation of a basic memory cell constructed using SR Flip-flop. (8)

15. a) With relevant examples, explain in detail about the various hazards in combinational and sequential circuits. Also discuss on how to design a hazard free circuit. (13)

(OR)

b) Write and verify the HDL structural description of the four-bit register with parallel load. Use a 2×1 multiplexer for the flip-flop inputs. Also include an asynchronous clear input. (13)

PART – C (1×15=15 Marks)

16. a) Construct an ASM chart for a digital system that counts the number of people in a room. People enter the room from one door with a photocell that changes a signal 'x' from 1 to 0 when the light is interrupted. They leave the room from a second door with a similar photocell with a signal 'y'. Both 'x' and 'y' synchronized with the clock, but they may stay on or off for more than one clock-pulse period. The data processor subsystem consists of an up-down counter with a display of its contents. (15)

(OR)

b) A traffic light is installed at a junction of a railroad and a road. The traffic light is controlled by two switches in the rails placed one mile apart on either side of the junction. A switch is turned on when the train is over it and turned off otherwise. The traffic light changes from green (logic-0) to red (logic-1) when the beginning of the train is one mile from the junction. The light changes back to green when the end of the train is one mile away from the junction. Assume that the length of the train is less than two miles.

i) Obtain the primitive flow table for the circuit.

ii) Show that the flow table can be reduced to four rows. (15)

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