Reg. No. :

Question Paper Code : X20440

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2020
AND APRIL/MAY 2021
Third Semester
Electronics and Communication Engineering
EC 6302 – DIGITAL ELECTRONICS
(Common to Mechatronics Engineering and Robotics and Automation Engineering)
(Regulations 2013)
(Also Common to PTEC 6302 – Digital Electronics for B.E. Part-Time – Second Semester – Electronics and Communication Engineering – Regulations 2014)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. Convert $Y = A + B\overline{C} + AB + \overline{A}BC$ into canonical form.

2. State the advantages of CMOS logic.

3. Define Half adder and full adder.

4. What is priority Encoder ?

5. Define race around condition in flip flop.

6. Draw D-latch with truth table.

7. Give the classification of programmable logic devices.

8. How the bipolar RAM cell is different from MOSFET RAM cell ?

9. What are the steps for the analysis of asynchronous sequential circuit ?

10. What is the significance of state assignment ?

PART – B **(5×13=65 Marks)**

11. a) i) Find the MSOP representation for $F(A, B, C, D, E) = m(1, 4, 6, 10, 20, 22, 24, 26) + d(0, 11, 16, 27)$ using K-Map method. Draw the circuit of the minimal expression using only NAND gates. **(7)**

ii) With neat circuit diagram, explain the function of 3-input TTL NAND gate. **(6)**

(OR)

b) What are the advantages of using tabulation method ? Determine the Minimal sum of products for the Boolean expression $F = \Sigma(1, 2, 3, 7, 8, 9, 10, 11, 14, 15)$ using tabulation method. **(13)**

12. a) i) Design a 4 ∗ 1 multiplexer circuit. **(7)**

ii) Implement the function using multiplexer $F = \Sigma(0, 1, 3, 4, 8, 9, 15)$. **(6)**

(OR)

b) i) Draw the logic diagram of Binary to octal decoder and explain the working in detail. **(7)**

ii) How is the carry look ahead adder faster than a ripple carry adder ? Explain in detail with neat sketches. **(6)**

13. a) Design and explain the working of a synchronous mod-3 counter. **(13)**

(OR)

b) Using SR flip-flops design a parallel counter which counts in the sequence 000, 111, 101, 110, 001, 010, 000,... **(13)**

14. a) i) Implement the following function using PLA. **(10)**

$F_1(x, y, z) = \Sigma\, m(1, 2, 4, 6)$

$F_2(x, y, z) = \Sigma\, m(0, 1, 6, 7)$

$F_3(x, y, z) = \Sigma\, m(2, 6)$

ii) Write short notes on FPGA. **(3)**

(OR)

b) i) Explain memory READ and WRITE operation with neat timing diagram. **(7)**

ii) Explain the organization of ROM with relevant diagrams. **(6)**

15. a) Design a asynchronous sequential circuit with 2 inputs T and C. The output attains a value of 1 when T = 1 and C moves from 1 to 0. Otherwise the output is 0.

(OR)

b) Explain the different methods of Race Free State assignment.

PART – C **(1×15=15 Marks)**

16. a) A sequential circuit has two JK flip-flops A and B, two inputs x and y and one output z. The flip-flop input equations and circuit output equations are :

$J_A = Bx + B'y'$ $K_A = B'xy'$

$J_B = A'X$ $K_B = A + xy'$

$z = Ax'y' + Bx'y'$

i) Draw the logic diagram of the circuit.

ii) Tabulate the state table.

iii) Derive the state equations for A and B.

(OR)

b) Write briefly on FPGA. Compare the advantages of a digital controller using FPGA and using discrete IC devices.