Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 20410

B.E/B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2018.

Third Semester

Electronics and Communication Engineering

EC 6304 — ELECTRONIC CIRCUITS – I

(Regulations 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Why is FET known as Voltage variable resistor?

2. What do you meant by thermal runaway?

3. What is the need of differential amplifier?

4. What is meant by bootstrapping?

5. Calculate the output resistance of a source -follower circuit. Given that

   $R_s = 0.75\ \text{k}\Omega$, $r_o = 12.5\ \text{k}\Omega$, and $g_m = 11.3$ mA/V.

6. Draw the low frequency equivalent circuit of FET.

7. What is Miller Effect? What is the effect of Millers capacitance on the frequency response of an amplifier?

8. Define Unity gain frequency (f_T) and Beta cutoff frequency (f_β).

9. Draw the MOSFET current source circuit.

10. Mention the advantage of NMOS amplifier with depletion load than NMOS amplifier with enhancement load.

PART B — (5 × 13 = 65 marks)

11. (a) (i) With relevant circuit diagram, explain the voltage divider bias of n-channel JFET. (6)

(ii) Determine the Q-point values of I_C and V_{CE} for the circuit in Figure 1. Assume V_{CE} = 8 V, R_B = 360 kΩ and R_C = 2 kΩ. Also construct the dc load line and plot the Q-point (7)

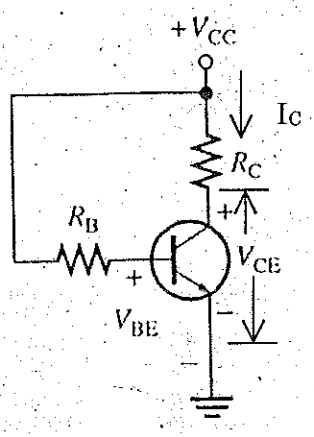

Figure 1

Or

(b) (i) Explain the methods employed for Bias compensation and thermal stability of transistor circuits. (6)

(ii) Determine V_{CE} and I_C in the voltage-divider biased transistor circuit given in Figure 2. Assume $V_{cc} = 20\,V$, $R_1 = 6.8k\Omega$, $R_2 = R_C = R_E = 1k\Omega$, $\beta_{DC} = 50$ and $I_E = I_B + I_C$. Assume $V_{BE} = 0.7V$. (7)

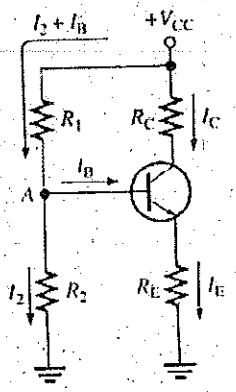

Figure 2

12. (a) Draw the circuit diagram of a Common Emitter amplifier with voltage divider bias, coupling capacitor and bypass capacitor. With the help of small-signal equivalent circuit, obtain the expression for voltage gain, current gain, input and output impedance. (13)

Or

PART B — (5 × 13 = 65 marks)

11. (a) (i) With relevant circuit diagram, explain the voltage divider bias of n-channel JFET. (6)

(ii) Determine the Q-point values of Ic and V_{CE} for the circuit in Figure 1. Assume V_{CE} = 8 V, R_B = 360 kΩ and R_C = 2 kΩ. Also construct the dc load line and plot the Q-point (7)

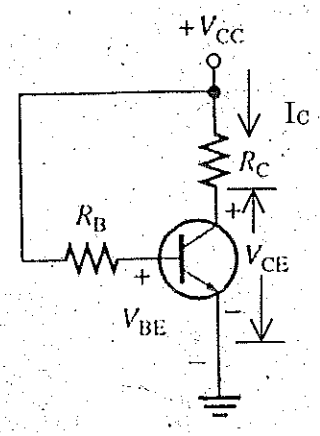

Figure 1

Or

(b) (i) Explain the methods employed for Bias compensation and thermal stability of transistor circuits. (6)

(ii) Determine V_{CE} and Ic in the voltage-divider biased transistor circuit given in Figure 2. Assume $V_{cc} = 20\,V$, $R_1 = 6.8k\Omega$, $R_2 = R_C = R_E = 1k\Omega$, $\beta_{DC} = 50$ and $I_E = I_B + I_C$. Assume $V_{BE} = 0.7V$. (7)

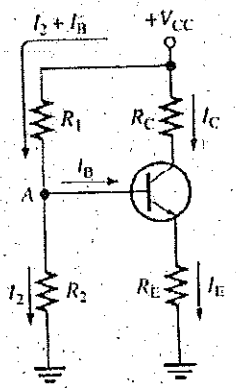

Figure 2

12. (a) Draw the circuit diagram of a Common Emitter amplifier with voltage divider bias, coupling capacitor and bypass capacitor. With the help of small-signal equivalent circuit, obtain the expression for voltage gain, current gain, input and output impedance. (13)

Or

(b) (i) With relevant circuit diagrams, explain the differential amplifier applied with common mode voltage and differential mode voltage. (8)

(ii) Draw the h-parameter model of Common emitter NPN transistor and obtain its h-parameters. (5)

13. (a) (i) Draw the small signal equivalent circuit of NMOS source follower. Also obtain the expression for the gain. (8)

(ii) With relevant circuit diagram, explain cascode NMOS amplifier circuit. (5)

Or

(b) Determine the small-signal voltage gain of a JFET amplifier. Consider the circuit shown in Figure 3 with transistor parameters : I_{DSS} = 12 mA, V_P = –4 V and λ = 0.008 V^{-1}. Also draw the Small-signal equivalent circuit of common source JFET, assuming bypass capacitor acts as a short circuit. (13)

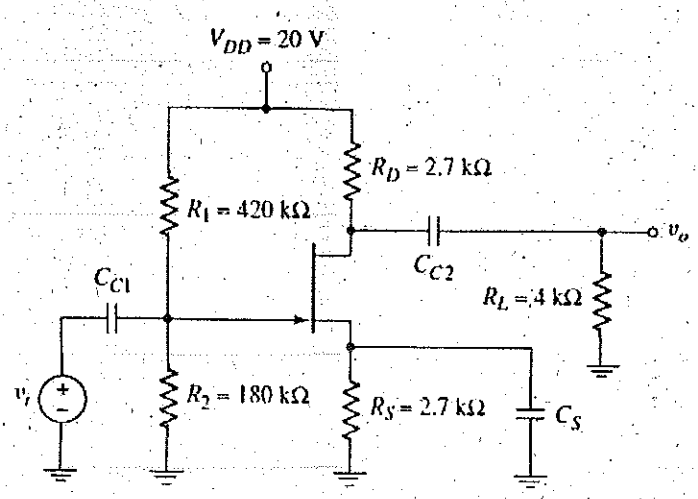

Figure 3

14. (a) (i) Draw the small signal equivalent circuit of common emitter circuit including the equivalent Miller capacitance. Also derive the expression for the Miller Capacitance. (8)

(ii) Calculate the bandwidth f_β and capacitance C_π of a bipolar transistor. Consider a bipolar transistor that has parameters f_T = 20 GHz at I_C = 1 mA, β_0 = = 120, $C\mu$ = 0.08 pF, V_T = 0.026V, and g_m = 38.5mA/V. (5)

Or

(b) (i) Derive the expression for beta cut off frequency. (5)

(ii) Determine the 3 dB frequency of an emitter-follower amplifier circuit with an output coupling capacitor. Consider the circuit shown in Figure 4 with transistor parameters β = 100, $V_{BE(on)}$ = 0.7V, and V_A = 120 V. The output Coupling capacitance is $C_{C2} = 1\ \mu F$, I_{CQ} = 0.838 mA. The small-signal parameters are: r_π = 3.10 $k\Omega$, g_m = 32.2 mA/V, and r_o = 143 $k\Omega$. (8)

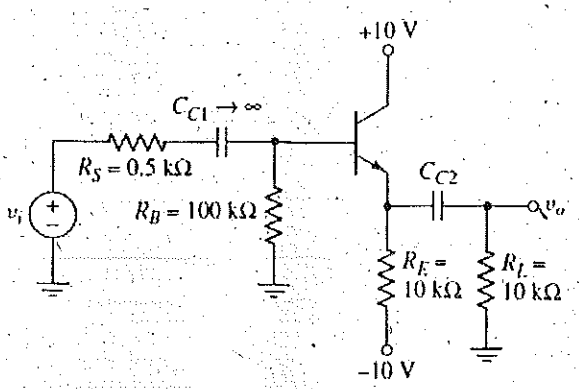

Figure 4

15. (a) (i) With relevant circuit diagrams, explain the working of NMOS amplifier with depletion load. Also obtain the expression for small voltage gain. (8)

(ii) Draw the small signal equivalent circuit of NMOS inverter with enhancement load device. Also obtain the small signal voltage gain. (5)

Or

(b) (i) With relevant circuit diagram and equivalent circuit diagram, determine the voltage gain of CMOS common-source amplifier. (8)

(ii) Determine the small signal voltage gain of the CMOS common source amplifier given in Figure 5. Assume transistor parameters of $V_{TN} = +0.8V$, $V_{TP} = -0.8\,V$, $k'n = 80\ \mu A/V^2$, $k'_p = 40\ \mu A/V^2$, $(W/L)_n = 15$. $(W/L)_p = 30$, and $\lambda_n = \lambda_p = 0.01V^{-1}$. Also, assume $I_{Bias} = 0.2\,mA$. (5)

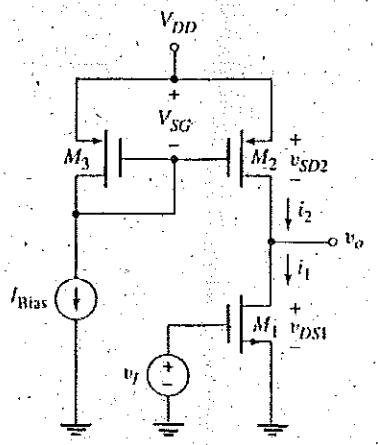

Figure 5

PART C — (1 × 15 = 15 marks)

16. (a) (i) The circuit in Figure 6 is to be used as a simple audio amplifier. Design the circuit such that the lower corner frequency is $f_L = 20$ Hz. (7)

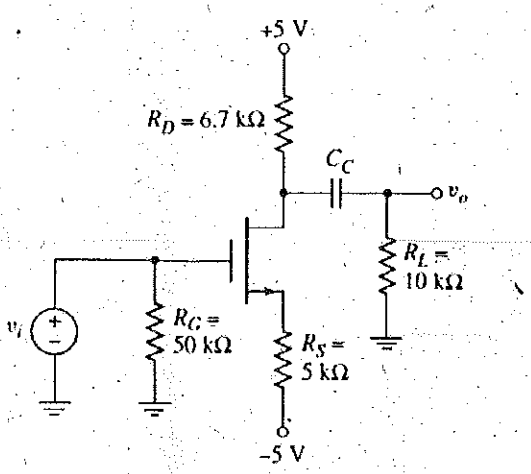

Figure 6

(ii) Design a bipolar amplifier to meet a set of specifications. The circuit configuration to be designed is shown in Figure 7 and is to amplify a 12 mV sinusoidal signal from a microphone to a 0.4 V sinusoidal output signal. $\beta = 100$, $V_{BE(on)} = 0.7$V, $V_A = \infty$. Assume that the output resistance of the microphone is 0.5 kΩ. (8)

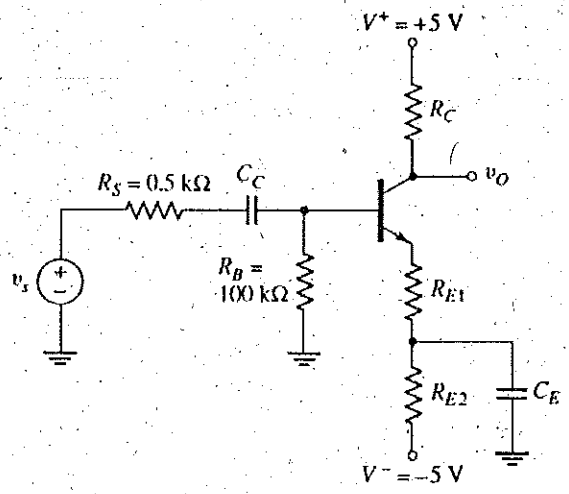

Figure 7

Or

(b) The design specifications of bipolar transistor audio amplifier are as follows. An audio amplifier is to deliver an average power of 0.1 W to an 8 Ω speaker from a microphone that produces a 10 mV peak sinusoidal signal and has a source resistance of 10 kΩ. Design has got three stages, namely input buffer stage, gain stage and output stage. Design the input buffer stage emitter follower and output stage emitter follower given in figure 8 (i) and 8 (i). (15)

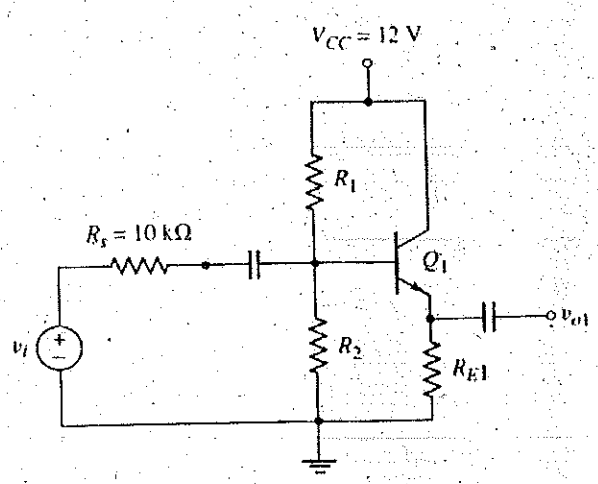

Figure 8 (i)

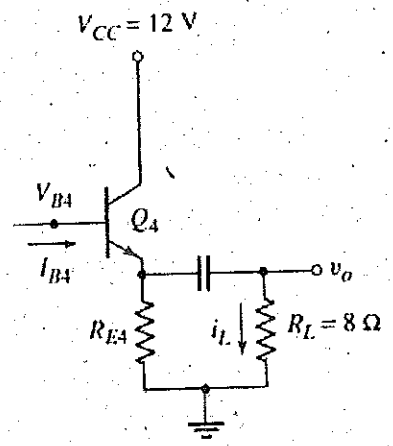

Figure 8 (ii)

Figure 8 (i) input buffer stage emitter follower and (ii) output stage emitter follower.